

5 BUS INTERFACE

The ETRAX 100LX bus interface has a 32/16-bit data bus, a 25-bit address bus, and six internally decoded chip select outputs. Six additional chip select outputs are multiplexed with other I/O functions, and are available in some configurations. The bus interface also supports either asynchronous or synchronous DRAM banks without external logic.

5.1 Data Bus

The 32-bit data bus provides support for 16-bit wide memories. The data bus is organized with the least significant byte at the lowest address (“little endian”).

The 32-bit data bus mode is shown in figure 5-1, and the 16-bit data bus mode is shown in figure 5-2 below:

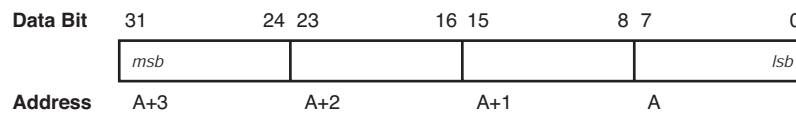


Figure 5-1 32-bit Mode Data Bus

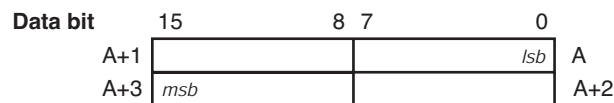


Figure 5-2 32-bit Wide Data on a 16-bit Mode Data Bus

5.2 Bus Interface Registers

Register	Function
R_WAITSTATES	A 32-bit write only register containing waitstate settings for peripheral, SRAM, and flash-PROM chip selects.
R_BUS_CONFIG	A 32-bit write only register for selecting bus width, common write enable (cwe) or <i>bytewise</i> write enable (bwe) selection, and DMA burst length. It is also used for setting write delay mode for chip selects.
R_BUS_STATUS	A 32-bit read only register that shows the initial values of the bus status pins bs0 - bs3 after reset.
R_DRAM_TIMING	A 32-bit write only register for asynchronous DRAM waitstate configuration.
R_SDRAM_TIMING	A 32-bit write only register for SDRAM enabling and configuration.
R_DRAM_CONFIG	A 32-bit write only register for asynchronous DRAM bus width, and DRAM type and bank selection.
R_SDRAM_CONFIG	A 32-bit write only register for SDRAM bus width, and SDRAM type and bank selection.

Table 5-1 Bus Interface Registers

For more detailed information see chapter 18.2 *Bus Interface Configuration Registers*.

5.3 Address and Chip Selects

The ETRAX 100LX chip operates with a 32-bit wide address space internally, but only address bits 25-1 are available on the external pins. Address bits 30-26 are decoded internally to generate the different memory chip select outputs, and the select of DRAM banks and internal I/O. Address bit 31 is used to select whether the cache is used or bypassed by CPU accesses. Additional chip selects are configured in the register R_PORT_PB_SET (See chapter 18.2 *Bus Interface Configuration Registers*).

The addresses are decoded to generate chip selects as follow:

Address Range (hex)	Size (Mbyte)	Name	Description
00000000-03FFFFFF	64	cse0	EPROM/flash PROM bank 0 chip select (Note: 1)
04000000-07FFFFFF	64	cse1	EPROM/flash PROM bank 1 chip select (Note: 1)
08000000-0BFFFFFF	64	csr0	SRAM bank 0 chip select. (Note: 1)
0C000000-0FFFFFFF	64	csr1	SRAM bank 1 chip select (Note: 1)
10000000-13FFFFFF	64	csp0	Peripheral chip select 0 (Note: 1)
14000000-17FFFFFF	64	csp1	Peripheral chip select 1 (Note: 1) Note: 2)
18000000-1BFFFFFF	64	csp2	Peripheral chip select 2 (Note: 1) (Note: 2)
1C000000-1FFFFFFF	64	csp3	Peripheral chip select 3 (Note: 1) (Note: 2)
20000000-23FFFFFF	64	csp4	Peripheral chip select 4 (Note: 2)
24000000-27FFFFFF	64	csp5	Peripheral chip select 5 (Note: 1) (Note: 2)
28000000-2BFFFFFF	64	csp6	Peripheral chip select 6 (Note: 1) (Note: 2)
2C000000-2FFFFFFF	64	csp7	Peripheral chip select 7 (Note: 1) (Note: 2)
30000000-3FFFFFFF	256	-	Do not use (Note: 3)
40000000-7FFFFFFF	1024	-	DRAM interface (Note: 1)
80000000-AFFFFFFF	768		Same as 00000000-2FFFFFFF but uncached
B0000000-B7FFFFFF	128	-	Internal registers
B8000000-BFFFFFFF	128	-	Internal start up code
C0000000-FFFFFFF	1024	-	Same as 40000000-7FFFFFFF but uncached

Table 5-2 *Chip Selects*

- Note 1:** Add 80000000 (hex) to bypass the cache.
- Note 2:** Peripheral select 1 - 3 and 5 - 7 are multiplexed with bits 2 - 7 in general port PB in the I/O block, and are not available if these pins are configured as general port pins.
- Note 3:** This region is internal registers and start-up code, but it is cached. Never use this area for accessing internal registers.

5.4 Internal Bus Arbitration

The bus interface performs the bus arbitration between the possible internal bus masters. The bus priority order is:

- 1 Shared RAM interface (*highest priority*)
- 2 External DMA channels
- 3 DRAM refresh
- 4 Internal DMA channels
- 5 CPU and cache (*lowest priority*)

5.5 Bus Width, Cycle Timing and Wait States

The bus interface supports 4 asynchronous DRAM banks, 8 synchronous DRAM banks (i.e. 2 groups of SDRAM banks with 2 to 4 banks per group), and between 6 to 12 other memory banks depending on its configuration. Each memory bank is connected to one of the chip select outputs. The banks are separated into five groups:

Group 1	$\overline{cse0}, \overline{cse1}$
Group 2	$\overline{csr0}, \overline{csr1}$
Group 3	$\overline{csp0}, \overline{csp1}, \overline{csp2}, \overline{csp3}$
Group 4	$\overline{csp4}, \overline{csp5}, \overline{csp6}, \overline{csp7}$
Group 5	DRAM banks

Table 5-3

The ETRAX 100LX bus width and number of wait states can be configured individually for each group. The bus width can be configured to either 16 or 32 bits using the internal register R_BUS_CONFIG. All banks in the same group have the same width. For group 1, the EPROM/flash PROM group, the initial bus width is decided by bus status pin 0 (**bs0**) at system reset. If **bs0** is low, the bus width is configured to 16 bits. If **bs0** is high, then the bus width is configured to 32 bits.

All bus cycles are run in consecutive bursts, with a maximum length of 32 bytes, and a minimum length of 1 byte. A burst will never cross a 32-byte boundary. A burst is either read or write, and the data direction is never changed within a burst.

For each group of memory banks except Synchronous DRAM banks, the following wait state parameters can be configured:

Parameter	Name	Size (bits)	Description
Early wait states	ew	2	Number of wait states before the falling edge of \overline{rd} , $\overline{wr0} - \overline{wr3}$, or \overline{cas} .
Late wait states	lw	2 or 4 (Note: 44)	Number of wait states after the falling edge of \overline{rd} , $\overline{wr0} - \overline{wr3}$, or \overline{cas} .
Turn-off wait states	zw	2	Number of wait states after the end of a burst. The turn-off wait states of the ending burst and the early wait states of the next burst may overlap.

Table 5-4 Memory Bank Wait State Parameters That Can Be Configured

Note 4: There are 2 bits for DRAM, and 4 bits for all other memory banks.

Group or Cycle	Wait State Ranges		
	Early	Late	Turn Off
Group 1: $\overline{cse0}$, $\overline{cse1}$	0 – 3	0 – 15	0 – 3
Group 2: $\overline{csr0}$, $\overline{csr1}$	0 – 3	0 – 15	0 – 3
Group 3: $\overline{csp0}$, $\overline{csp1}$, $\overline{csp2}$, $\overline{csp3}$	0 – 3	0 – 15	0 – 3
Group 4: $\overline{csp4}$, $\overline{csp5}$, $\overline{csp6}$, $\overline{csp7}$	0 – 3	0 – 15	0 – 3
Asynchronous DRAM \overline{cas} cycle	0 – 3	0 – 3	0 – 3
Asynchronous DRAM \overline{ras} cycle	0 – 3	0 – 3	–
Asynchronous DRAM \overline{ras} precharge cycle	–	0 – 3	–

Table 5-5 Possible Wait State Settings

Wait states for groups 1 to 4 are configured in R_WAITSTATES, and asynchronous DRAM wait states are configured in R_DRAM_TIMING. A zero wait state bus cycle lasts 20 ns. Between bursts there are 10 ns. Each wait state adds 10 ns to the bus cycle time. Default after reset is maximum number of wait states.

For Synchronous DRAM banks, the following wait state parameters can be configured:

Parameter	Name	Size (bits)	Description
Master clock select	clk100	1	Synchronous DRAM master clock select. Possible configuration is either 50 MHz or 100 MHz.
\overline{cas} latency cycles	cl	2	Number of delay cycles from read bank command to valid read data.
\overline{ras} to \overline{cas} delay cycles	rcd	2	Number of delay cycles after activate bank command.
\overline{ras} precharge delay cycles	rp	2	Number of delay cycles after precharge bank command.
Row cycle time	rc	2	Auto refresh cycle time.
Power down exit delay	pde	1	Number of delay cycles from power down exit to new command.

Table 5-6 SDRAM Bank Wait State Parameters That Can Be Configured

Table 5-7 below gives possible Synchronous DRAM wait state settings and corresponding delay cycles for both a 50 and 100 MHz master clock:

Cycle	Wait State Ranges		Delay Cycle Ranges	
	50 MHz	100 MHz	50 MHz	100 MHz
\overline{cas} latency	1 - 2	0 - 1	2 - 3	2 - 3
\overline{ras} to \overline{cas} delay	0 - 3	0 - 3	1 - 4	2 - 5
\overline{ras} precharge delay	0 - 3	0 - 3	1 - 4	2 - 5
Row cycle time	0 - 3	0 - 3	6 - 9	6 - 9
Power down exit delay	0 - 1	0 - 1	1 - 2	1 - 2

Table 5-7 Possible Wait State Settings and Delay Cycles for Synchronous DRAM

A delay cycle lasts 20 ns when a 50 MHz SDRAM system clock is selected, and 10 ns when a 100 MHz system clock is selected.

5.6 Memory Timing

The timing for the read cycles, both with and without early wait states, is shown in the figure below. This timing diagram is valid for SRAM, flash and peripheral devices.

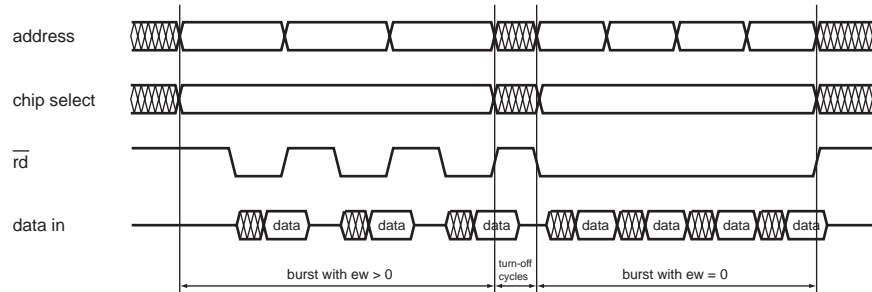


Figure 5-3 Read Cycles for SRAM, Flash Memory and Peripheral Devices.

5.7 Write Modes

5.7.1 Normal and Extended Write Mode

During a normal ETRAX 100LX write cycle, the $\overline{wr0} - \overline{wr3}$ strobes will go high 5 ns before the end of the bus cycle. The write pulses can be extended to the end of the bus cycle. Normal and extended write mode can be configured individually for each of the groups, 1 to 4, of the memory banks in R_BUS_CONFIG. Asynchronous DRAM is configured in R_DRAM_TIMING.

5.7.2 Bytewise and Common Write Enable Mode

The memory banks in group 2, the SRAM group, can be configured with R_BUS_CONFIG to use either four bitwise write enable strobes or one common write enable strobe. In bitwise write enable mode, bwe, four write strobes are available, one for each byte in the data bus. In common write enable mode, cwe, one common write enable strobe and four byte enable strobes are available. The byte enable strobes are active during both read and write cycles. In 32-bit cwe mode, one of the byte enable strobes is output on the unused address bit 1.

16/32-bit bwe	32-bit cwe	16-bit cwe
$\overline{wr0}$	$\overline{be0}$	$\overline{be0}$
$\overline{wr1}$	$\overline{be1}$	$\overline{be1}$
$\overline{wr2}$	$\overline{be2}$	-
$\overline{wr3}$	\overline{we}	\overline{we}
a1	$\overline{be3}$	a1

Table 5-8 Pin Assignment for Bytewise and Common Write Enable Modes

Note 5: For information regarding actual pin assignments see chapter 19 *Electrical Information*.

The byte enable strobes, $\overline{be0} - \overline{be3}$, have the same timing as the address bus. The write enable strobe, \overline{we} , has the same timing as the write strobes, $\overline{wr0} - \overline{wr3}$.

5.8 External Interrupt Acknowledge

If the external interrupt is configured for an external vector number, an interrupt acknowledge cycle will occur when the interrupt is granted. During the interrupt acknowledge cycle, an 8-bit vector number is read on the low byte of the data bus. The cycle is indicated by the $\overline{\text{inta}}$ signal going low, and $\overline{\text{rd}}$ and $\overline{\text{wr}}$ are high during the cycle. The address and chip selects are undefined. Maximum timing is used for the $\overline{\text{inta}}$ cycle, regardless of setting: $\text{ew} = 3$, $\text{lw} = 15$, and $\text{zw} = 3$.

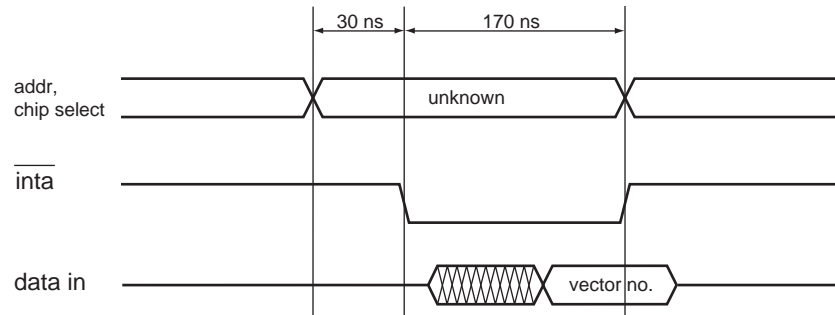


Figure 5-4 External $\overline{\text{inta}}$ Cycle

Note 6: For more information see chapter 19 *Electrical Information*.

5.9 Access to Internal I/O

Data read from or written to an internal I/O unit is present on the data bus for 2 clock cycles (i.e. 20 ns). The $\overline{\text{rd}}$ pulse is active for 20 ns and the $\overline{\text{wr}}$ pulses are active for 10 ns. All chip selects are inactive.

5.10 Wait Input and Bus Cycle Rerun

An external wait pin ($\overline{\text{wait}}$) is provided, and can be used by external devices to insert extra wait states. The $\overline{\text{wait}}$ input is fully synchronized, and $\overline{\text{wait}}$ is sampled 3 clock cycles (30 ns) before the end of the bus cycle. As a result, the use of the $\overline{\text{wait}}$ input requires that the number of internal wait states ($\text{ew} + \text{lw}$) for the memory area in question to be set to 3 or more.

If the $\overline{\text{wait}}$ input is active for too long, it can cause overrun/underrun errors (e.g. in the network interface). The maximum allowed active time is, therefore, limited depending on the application.

For very slow external units it is possible to make a bus cycle rerun. However, this only applies for non-cacheable CPU accesses and is not allowed to be used on other types of cycles, like DMA cycles etc. The rerun input is sampled at the rising edge of the $\overline{\text{wait}}$ signal. If the rerun input is sampled low, the CPU will rerun the bus cycle.

5.11 DRAM Interfaces

The DRAM interface can be configured to use *Asynchronous DRAMs* (EDO or Fast Page Mode), *Synchronous DRAMs* (SDRAM), or *Double Data Rate Synchronous DRAMs* (DDR SDRAM).

Selection between asynchronous and synchronous modes is made by the **sdram** mode bit in the R_DRAM_TIMING register. When this mode bit is not set (**sdram** = 0), the asynchronous DRAM mode is enabled and the registers: R_DRAM_TIMING and R_DRAM_CONFIG are used for configuration.

When the **sdram** mode bit is set (**sdram** = 1) in R_DRAM_TIMING, the SDRAM mode is enabled and R_SDRAM_TIMING and R_SDRAM_CONFIG are used for configuration.

ASYNC DRAM	SDRAM	DDR SDRAM
a25	$\overline{\text{sdram_ras}}$	$\overline{\text{sdram_ras}}$
a24	$\overline{\text{sdram_cas}}$	$\overline{\text{sdram_cas}}$
a23	$\overline{\text{sdram_we}}$	$\overline{\text{sdram_we}}$
$\overline{\text{ras0}}$	$\overline{\text{csd0}}$	$\overline{\text{csd0}}$
$\overline{\text{ras1}}$	$\overline{\text{csd1}}$	$\overline{\text{csd1}}$
$\overline{\text{ras2}}$	clk	clk
$\overline{\text{ras3}}$	cke	cke
cas<7.0>	dqm<7.0>	dqm<7.0>
$\overline{\text{dramwe}}$	-	dqs

Table 5-9 Pin Assignment for Asynchronous and Synchronous DRAM modes

Note 7: For information regarding actual pin assignments see *19 Electrical Information*.

The DRAM interface supports up to four banks of asynchronous DRAM chips and eight banks of Synchronous DRAM chips without external logic. 32-bit and 64-bit wide DRAM modules are supported as well as separate DRAM chips. DRAM bus width can be configured to 16 or 32 bits.

All DRAM accesses are performed in bursts. When the first access in a series of bursts is performed, the internal address is shifted down so that the row address appears on the lower pins of the address bus. The row address is stored in an internal register in ETRAX 100LX for later reference. When the row address portion of the cycle is finished, the column address is put on the address bus.

For every new burst, the row address is compared with the previously used row address that is stored in an internal register. If the row addresses are identical, the row address portion of the cycle can be left out which saves that time that would have been needed for the row access.

5.12 Asynchronous DRAM Interface

The ETRAX 100LX supports both Fast Page Mode and Hyper Page Mode (EDO) asynchronous DRAM chips. The timing diagram for a Fast Page Mode read cycle is shown in figure 5-5 below:

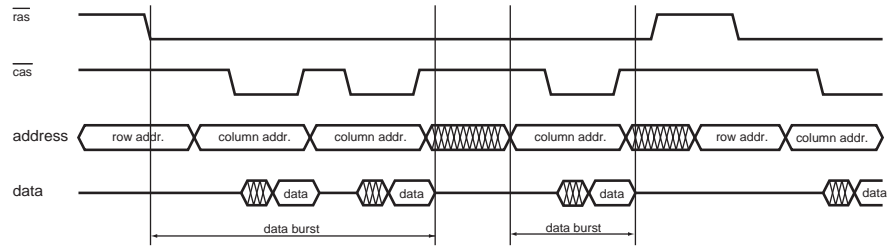


Figure 5-5 Timing Diagram for Fast Page Mode Read Cycles

If EDO DRAM chips are used, ETRAX 100LX uses the $\overline{\text{ras}}$ signal or the $\overline{\text{dramwe}}$ signal to tell the DRAM to release the data bus. The DRAM will release the data bus either when the $\overline{\text{ras}}$ signal goes high, or when the $\overline{\text{dramwe}}$ signal goes low.

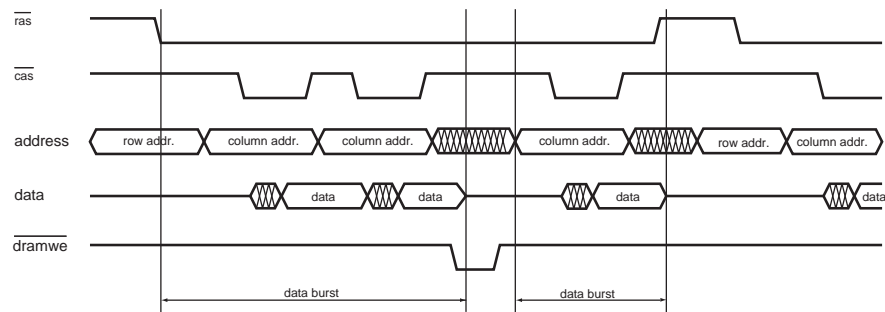


Figure 5-6 Timing Diagram for EDO Mode Read Cycles

5.12.1 Connecting the Asynchronous DRAM Banks

Four asynchronous DRAM banks are combined into two groups with two banks in each group. Both banks in one group must have the same number of column address bits.

When accessing these DRAM banks, the $\overline{\text{cas}}$ signals can be used either as bank strobes (bankwise $\overline{\text{cas}}$ mode), or as byte strobes (bytewise $\overline{\text{cas}}$ mode). One mode is used throughout a single application.

Bytewise $\overline{\text{cas}}$ mode is illustrated in figure 5-7 below. Only one $\overline{\text{ras}}$ signal at a time will be active in each group. The $\overline{\text{cas}}$ signals are used to select the different bytes within the word or dword.

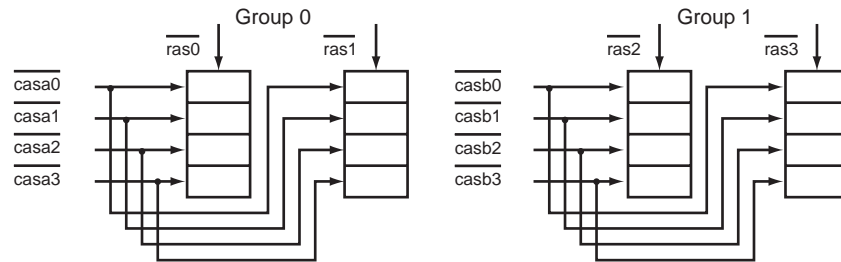


Figure 5-7 Bitwise $\overline{\text{cas}}$ Mode.

In a design using bankwise $\overline{\text{cas}}$ mode, as in figure 5-8, all the $\overline{\text{ras}}$ signals can be active simultaneously. $\overline{\text{casa}}$ decides which bank to access. If bitwise access is required, the byte $\overline{\text{cas}}$ signals are generated by gating $\overline{\text{casb}}$, used as byte enables, and $\overline{\text{casa}}$ as shown in figure 5-9.

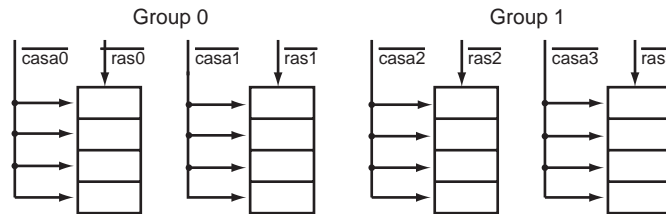


Figure 5-8 Bankwise Accessing of Asynchronous DRAM Modules.

Bankwise $\overline{\text{cas}}$ mode can be used without the $\overline{\text{cas}}$ gating if the software fulfills the following requirements:

- CPU accesses to DRAM area are always cached.
- All DMA descriptors are 32-bit aligned.
- A DMA data buffer and program code/data, or two different DMA data buffers, are not merged within the same 32-bit aligned dword.

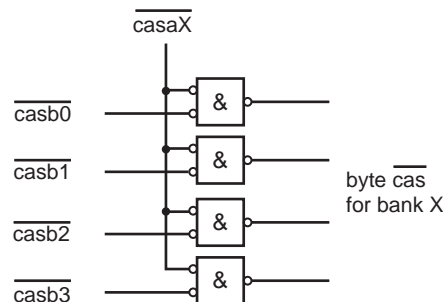


Figure 5-9 Generating Byte $\overline{\text{cas}}$.

When using 64-bit wide asynchronous DRAM modules, one $\overline{\text{ras}}$ signal is assigned to each bank and this signal controls all 64 bits. Only one $\overline{\text{ras}}$ is active at a time. The $\overline{\text{cas}}$ signals are used to select the different bytes within the word, see figure 5-10.

Upper and lower 32 bits are also tied together. In other words, bit 0 and bit 32 (bit 1 and bit 33, bit 2 and bit 34, etc.) are tied together, and one at a time they drive the databus.

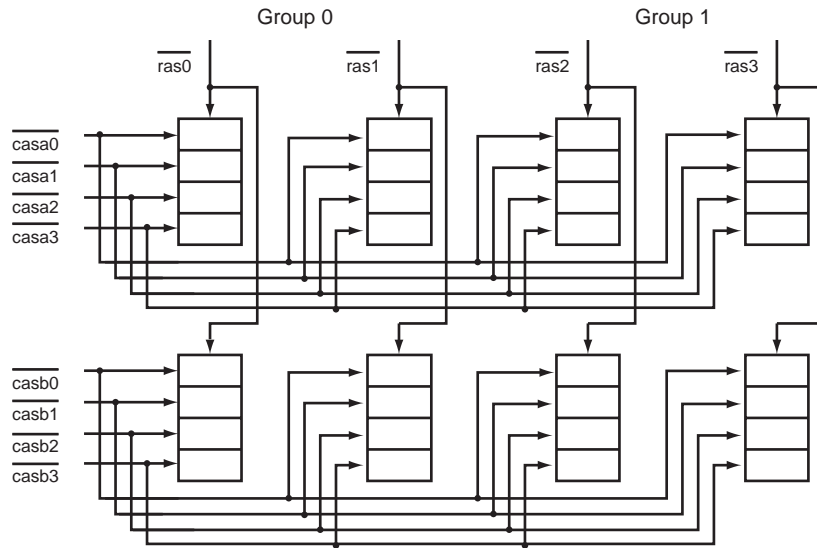


Figure 5-10 64-bit Wide Asynchronous DRAM Modules, All $\overline{\text{cas}}$ Signals Used For Selecting Bytes.

In bankwise mode with 64-bit wide modules, the $\overline{\text{cas}}$ signals are used to activate 32 bits at a time as shown in figure 5-11. In this case, all $\overline{\text{ras}}$ signals can be active at the same time, but it is not possible to select the separate bytes in the DRAM.

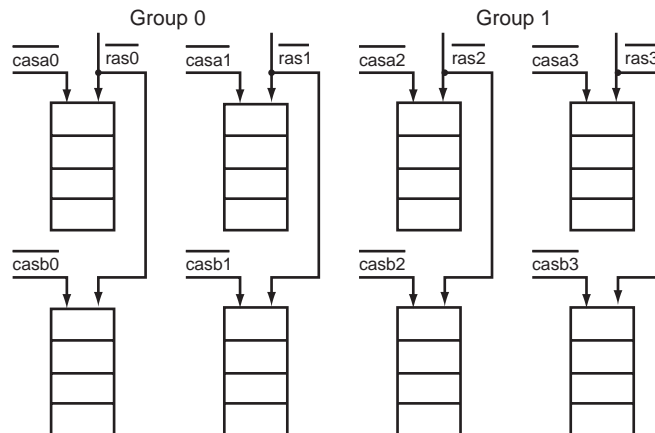


Figure 5-11 Bankwise Accessing, 64-bit Wide Asynchronous DRAM Modules.

5.12.2 Asynchronous DRAM Bank Configuration

Four asynchronous DRAM banks are combined into two groups with banks 0 and 1 in group 0, and banks 2 and 3 in group 1. The two banks in each group always share the same configuration from R_DRAM_CONFIG.

Common to all banks, the following configurations are available:

Width (1 bit)

Selects 16- or 32-bit DRAM bus width.

0	16-bit DRAM bus width.
1	32-bit DRAM bus width.

EDO or Fast page mode (1 bit)

0	Fast page mode.
1	EDO mode.

$\overline{\text{cas}}$ organization (1 bit)

0	The $\overline{\text{cas}}$ outputs are used for selecting bytes as in figure 5-7 or, if wide module mode is selected, as in figure 5-10.
1	One $\overline{\text{cas}}$ output for each bank, see figure 5-8 and figure 5-9, or if wide module mode is selected, two $\overline{\text{cas}}$ outputs per bank as in figure 5-11.

Group select mode (5 bits)

The group select mode determines how to select a group of DRAM banks:

Value	Select
0	Always select group 0.
1	Always select group 1.
2-8	Reserved.
9-29	The internal address bit number corresponding to the select mode value is used to select group.
30-31	Reserved.

The following configurations are available for each group individually:

Row Address Shift (3 bits)

During the $\overline{\text{ras}}$ portion of the cycle, the row portion of the internal address is shifted down to the lower address outputs to which the asynchronous DRAM address pins are connected. The value given decides how many steps the address bits are shifted:

Value	Shift
0	Internal address bits 29 - 9 shifted down to pins A21 - A1.
:	:
:	:
7	Internal address bits 29 - 16 are shifted down to pins A14 -A1, and pins A21 - A15 are set to 0 (zero).

(The internal address bits 25 - 22 are output on pins A25 - A22 during $\overline{\text{ras}}$ cycles.)

To accomplish the multiplexing of the row address and the column address on the address bus pins, the row address is shifted down to the lower pins of the bus during the $\overline{\text{ras}}$ portion of the bus cycle.

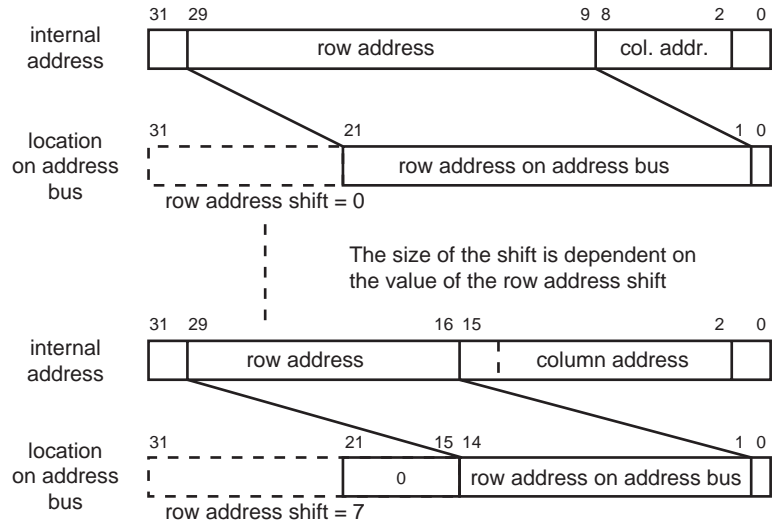


Figure 5-12 Row Address Shifting During the $\overline{\text{ras}}$ Portion of the Bus Cycle

Column Address Range (3 bits)

The column address range determines how many address bits that are used in the column address.

The ranges selected for the column address and the row address may overlap by one bit. When the row address has been shifted down, this bit corresponds to bit 1 on the address bus, which is not used in the 32-bit address. Consequently, the overlapping bit is part of the column address.

There may also be a gap between the row address and column address parts, which

are not used by the asynchronous DRAM bank. The bits in the gap can be used to select the bank and/or group.

In wide module mode, the selection between $\overline{\text{casa}}$ and $\overline{\text{casb}}$ is done by the highest address bit given by the column address range. The column address range should, in this case, be set to one higher than the actual highest column address bit to the DRAM.

Value	Column Address Bits
0	Up to and including address bit 8.
:	:
:	:
7	Up to and including address bit 15.

Bank Decode Mode (5 bits)

The bank decode mode determines how to select between the two banks in a group:

Value	Select
0	Always select bank 0 (group 0) or bank 2 (group 1).
1	Always select bank 1 (group 0) or bank 3 (group 1).
2-8	Reserved.
9-29	The internal address bit number corresponding to the decode mode value is used to select bank.
30-31	Reserved.

Wide Module Mode (1 bit)

This mode supports 64-bit wide asynchronous DRAM modules where all 64 bits are controlled by the same ras signal. Both casa and casb are used within both groups of DRAM banks.

If bankwise cas mode is combined with the wide module mode in any of the two groups, none of the groups can use casb as byte enables, see figure 5-11.

Value:	Select Mode:
0	Normal mode.
1	Wide module mode.

5.13 Synchronous DRAM Interface

The SDRAM interface can be configured to use a master clock of either 50 or 100 MHz. In 100MHz mode, the interface can also work as a DDR SDRAM interface. The maximum internal bus speed is always 50MHz regardless of the SDRAM master clock selection.

There is support for two groups of SDRAM banks. A group is the set of SDRAM banks that are collectively either 16, 32, or 64 data bits wide. The groups are controlled by the chip selects, csd0 and csd1 . Each group can be configured to use either two-bank or four-bank chips.

The timing for a 50 MHz SDRAM read cycle is shown in figure 5-13:

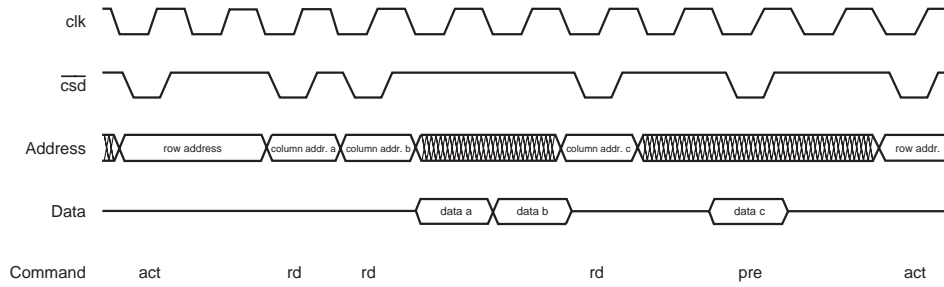


Figure 5-13 Timing Diagram for 50 MHz Read Cycles with \overline{cas} Latency and \overline{ras} Precharge Delay of 2 Delay Cycles

In 100MHz mode commands are only issued once every two clock cycles in order to maintain the internal bus speed of 50MHz.

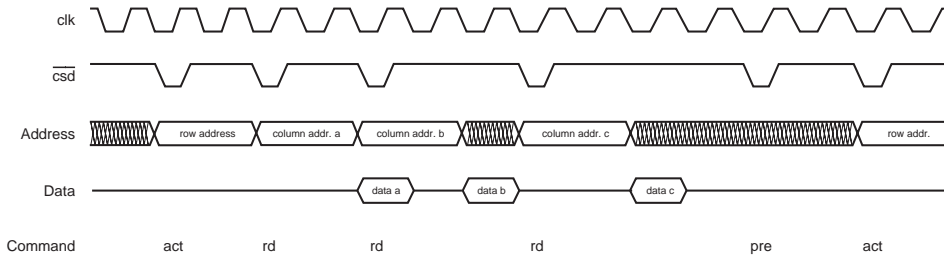


Figure 5-14 Timing Diagram for 100 MHz Read Cycles with \overline{cas} Latency and \overline{ras} Precharge Delay of 2 Delay Cycles

In DDR mode, a bi-directional data strobe, *dqs*, is used to qualify the data bus. The minimal burst length supported by DDR devices are two words and the second word is, therefore, masked during writes by the data mask, *dqm*, signals. Write latency for DDR devices is always set to one cycle.

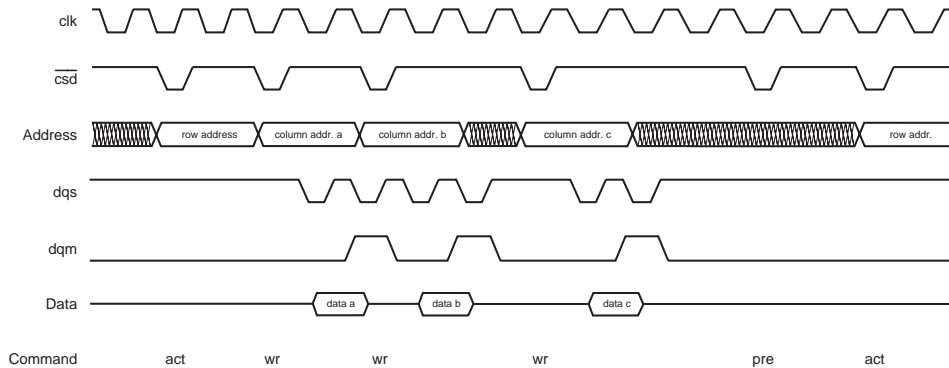


Figure 5-15 Timing Diagram for 100 MHz DDR Write Cycles

5.13.1 Power up and initialization

SDRAMs have an internal configuration register that must be written during initialization with the *mode register set* (mrs) command. The SDRAM must be in idle mode and the mrs command should, therefore, be preceded by an auto refresh cycle to make sure that the banks are pre charged. The mrs command is issued by writing to the cmd field in R_SDRAM_TIMING. During the mrs cycle, the mrs data field in R_SDRAM_TIMING is output on address bits 15 - 0. All bits in the mrs field should normally be set to zero except for the *cas* latency select bits.

It is possible to issue commands manually to the SDRAM by writing to the command field in R_SDRAM_TIMING. The possible commands are:

- precharge all banks
- auto refresh
- mode register set
- nop

All commands have to be followed by a nop command before a new command can be issued. Note that at least five CPU nop instructions should be inserted between each write to R_SDRAM_TIMING.

The manual commands should only be used during power up and initialization of the SDRAM banks. A typical initialization sequence is shown below:

- 1 Configure the banks by writing to R_SDRAM_CONFIG.
- 2 Configure the waitstate parameters and enable the master clock by writing to R_SDRAM_TIMING.
- 3 Wait for 200us.
- 4 Issue precharge all banks command by writing to the cmd field in R_SDRAM_TIMING.
- 5 Wait five CPU nop cycles.
- 6 Issue nop command by writing to the cmd field in R_SDRAM_TIMING.
- 7 Wait five CPU nop cycles.

Next, perform the following sequence eight times:

- 1 Issue auto refresh command by writing to the cmd field in R_SDRAM_TIMING.
- 2 Wait five CPU nop cycles.
- 3 Issue nop command by writing to the cmd field in R_SDRAM_TIMING.
- 4 Wait five CPU nop cycles.

Finally,

- 1 Issue mode register set command by writing to the cmd and mrs_data fields in R_SDRAM_TIMING.
- 2 Wait five CPU nop cycles.
- 3 Issue nop command by writing to the cmd field in R_SDRAM_TIMING.
- 4 Wait five CPU nop cycles.

5.13.2 Power save mode

It is possible to run the SDRAM interface in the Power save mode. In this mode, the SDRAM banks will enter Power save mode immediately after each auto refresh cycle. This is done by deasserting the cke signal. The SDRAM banks will remain in Power save mode until the next SDRAM bus request, or until they have to be refreshed again. There is a penalty of one or two delay cycles for each Power save mode exit. The Power save mode exit delay can be configured in R_SDRAM_TIMING.

5.13.3 100 MHz mode

It is possible to select a 100 MHz system clock together with both SDRAMs and DDR SDRAMs, but this will not give double the performance compared to the 50 MHz clock. Commands will only be issued every two cycles due to the internal 50 MHz bus speed. There will, however, be a speed-up since ras and cas latency will be shorter.

5.13.4 DDR mode

The DDR mode must be used with a 100 MHz system clock due to an internal DLL in the DDR SDRAM chips. Since the DDR SDRAMs only use the dqm signals as a data mask during write operations, 64-bit modules with one common chip select for all eight bytes can not be used.

5.13.5 Connecting the Synchronous DRAM banks

The Synchronous DRAM banks are combined into two groups where each group is controlled by a separate chip select signal.

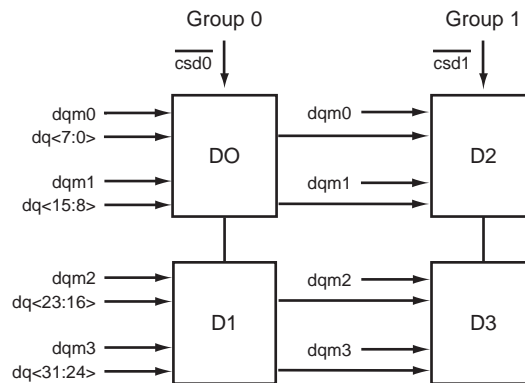


Figure 5-16 32-bit SDRAM Connection Comprising Four 16-bit SDRAM Devices.

When using 64-bit wide DRAM modules, one chip select is assigned to each group and controls all 64-bits. The eight dqm signals are used to select the different bytes within the word.

Upper and lower 32 bits are tied together. In other words, bit 0 and bit 32 (bit 1 and bit 33, bit 2 and bit 34, etc.) are tied together, and one at a time they drive the databus:

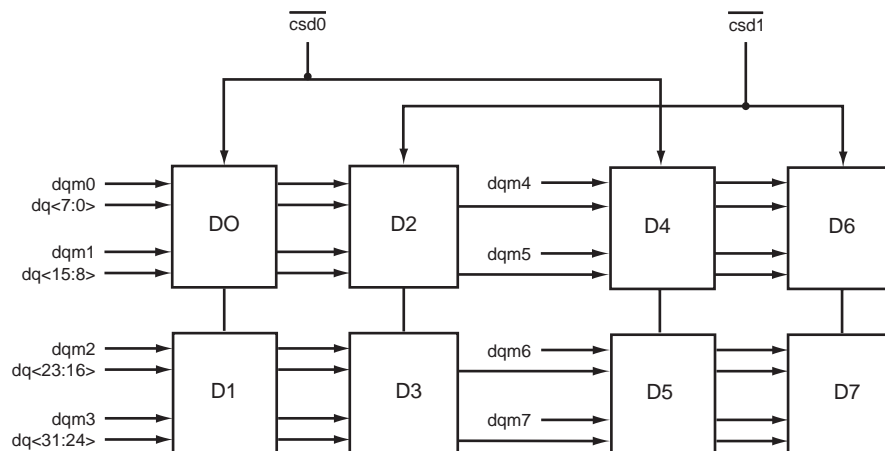


Figure 5-17 64-bit Wide SDRAM Module Comprising Eight 16-bit SDRAM Devices.

5.13.6 Synchronous DRAM Bank Configuration

SDRAM banks are combined into two groups where each group can use either two-bank or four-bank chips. The following configurations are common for all banks:

Width (1 bit)

Width selects either a 16- or 32-bit DRAM bus width.

Value	Select
0	16-bit DRAM bus width.
1	32-bit DRAM bus width.

Group Select Mode (5 bits)

The group select mode determines how to select a group of DRAM banks. When using only one group, the group select mode value must be set to either 0 or 1.

Value	Select
0	Always select group 0.
1	Always select group 1.
2-8	Reserved.
9-29	The internal address bit number corresponding to the select mode value is used to select group.
30-31	Reserved.

Row Address Shift (3 bits)

During activate bank commands, the row portion and the bank select bits are shifted down to the lower address outputs to which the DRAM address pins are connected. During precharge bank, read bank, and write bank commands, only the bank select bits are shifted down to the lower address outputs. When using two groups, both groups must have the same row address shift value.

The value given decides how many steps the address bus is shifted

Value	Shift
0	Internal address bits 29 - 9 are shifted down to pins A21 - A1.
:	:
:	:
7	Internal address bits 29 - 16 are shifted down to pins A14 - A1, and pins A21 - A15 are set to 0(zero).

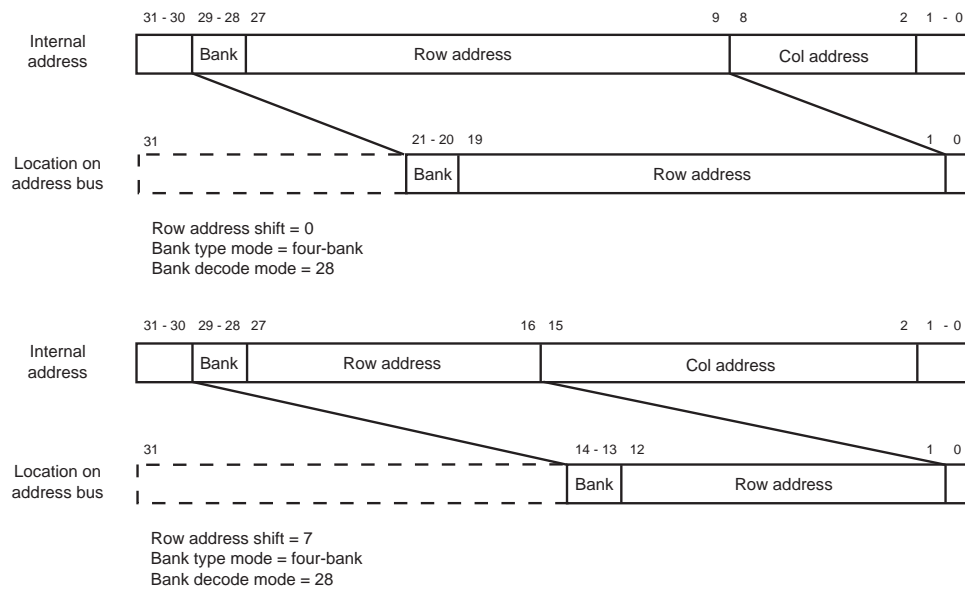


Figure 5-18 SDRAM Address Bus Shift During Activate Bank Commands

Column Address Range (3 bits)

The column address range determines how many address bits that are used in the column address.

The ranges selected for the column address and the row address may overlap by one bit. When the row address has been shifted down, this bit corresponds to bit 1 on the address bus, which is not used in the 32-bit address. Consequently, the overlapping bit is part of the column address.

There may also be a gap between the row address and column address parts, which are not used by the asynchronous DRAM chip. One bit in the gap can be used to select the group.

In wide module mode, the selection between $\overline{\text{casa}}$ and $\overline{\text{casb}}$ is done by the highest address bit given by the column address range. The column address range should, in this case, be set to one higher than the actual highest column address bit to the DRAM.

Address bit a10 on SDRAM chips is used to select auto precharging during read and write commands and is not used as a column address. In 32-bit mode, a10 will correspond to a12 on the ETRAX 100LX, and in 16-bit mode, a10 will correspond to a11. a10 is never used as an address bit during read and write commands. In configurations with more than 10 column addresses, the address continues on the next higher address bit after a10. When using two groups, both groups must have the same column address range value.

Value	Column Address Bits
0	Up to and including address bit 8.
:	:
:	:
7	Up to and including address bit 15.

The following configurations are available for each group individually:

Bank Type Mode (1 bit)

Bank type mode selects either the two-bank or four-bank mode:

Value	Select
0	Two-bank mode is selected.
1	Four-bank mode is selected.

Bank Decode Mode (5 bits)

The bank decode mode determines how to select between bank 0 and 1 in a group. In the four-bank mode, bank 2 and 3 will be selected by the next higher order address bit. The bank select bit or bits are shifted down to the lower address outputs according to the row address shift value.

Value	Column Address Bits
0 - 8	Reserved.
9 - 29	Internal address bit number corresponding to the decode mode value is used to select between bank 0 and 1.
30 - 31	Reserved.

Wide Module Mode (1 bit)

This mode supports 64-bit wide DRAM modules where all 64-bits are controlled by the same chip select signal. dqm0 to dqm7 are used to control the individual bytes within both groups of DRAM banks.

Value:	Select Mode:
0	Normal mode
1	Wide module mode