9 NETWORK INTERFACE

The ETRAX 100LX includes an on-chip Fast Ethernet controller.

The ETRAX 100LX network interface supports 10 and 100 Mbps Ethernet (IEEE 802.3 and Ethernet II) protocols. With 10 Mbps, the physical interface can be configured to be compatible with either 802.3 MII or SNI (National Semiconductor DP8391 compatible interface). 100 Mbps is only supported over 802.3 MII.

The network interface has the following features:

- 10 MBit/100 MBit MII Interface
- 10 MBit Serial Network Interface (SNI)
- Support for full duplex including pause frames
- 2 simultaneous station addresses

9.1 The Ethernet II and IEEE 802.3 Standards

There are some minor differences between the IEEE 802.3 standard and Ethernet II regarding frames. Figure 9-1 below shows the frame format for the Ethernet II standard and the frame format for the IEEE 802.3 standard.

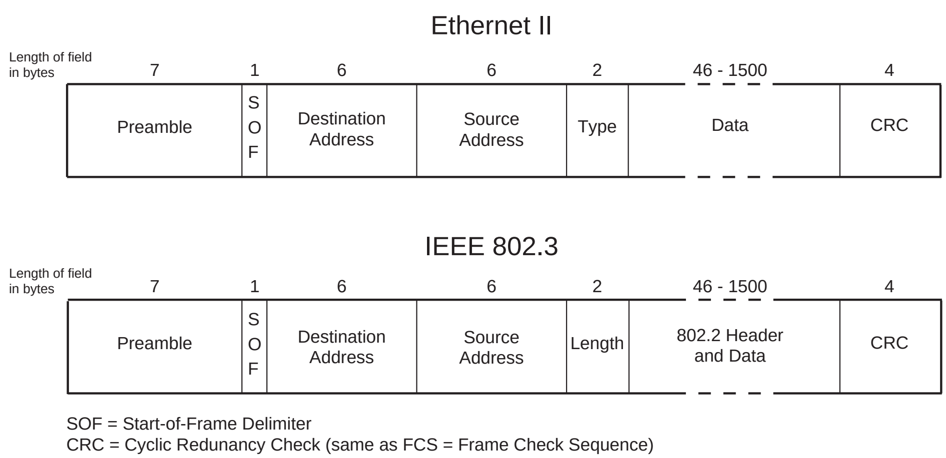

Figure 9-1 A description of the frames in Ethernet and the IEEE 802.3 standard

Table 9-1 below gives short explanations of the frames' contents:

Frame fields	Description	Length (bytes)
Preamble	Provides synchronization. Consists of 7 bytes of the bit pattern "10101010".	7
Start-of-Frame Delimiter (SOF)	Provides framing. Contains the bit pattern "10101011".	1
Destination Address	The address of the destination station. The first bit indicates: 0 = individual; 1 = group address	6
Source Address	The address of the sending station.	6
Length or type	Specifies the length or type of the data field.	2
Data	The data content.	46 - 1500
Pad	If the actual data is less than 46 bytes, pad bytes consisting of zeros are added to it up to the required minimum of 46 bytes.	0 - 46
CRC	Used for error checking at the destination station. (CRC = Cyclic Redundancy Check)	4

Table 9-1 Ethernet frame contents

9.2 Network interface registers

Table 9-2 below provides a brief description of the network interface registers. For more detailed information, see 18.9 *Network Interface Registers*.

Register	Function
R_NETWORK_SA_0	A 32-bit wide write only register which contains the bit address [31:0] of station address MA0.
R_NETWORK_SA_1	A 32-bit wide write only register which contains the bit address [15:0] of station address MA1, and the bit address [47:32] of station address MA0.
R_NETWORK_SA_2	A 32-bit wide write only register which contains the bit address [47:16] of station address MA1.
R_NETWORK_GA_0	A 32-bit wide write only register which contains the bit [31:0] of the group address table.
R_NETWORK_GA_1	A 32-bit wide write only register which contains the bit [63:32] of the group address table.
R_NETWORK_REC_CONFIG	A 32-bit wide write only register for configuration of the Ethernet receiver.
R_NETWORK_GEN_CONFIG	A 32-bit wide write only register for internal loop back, setting the frame format, SNI and MII mode selection, and enabling/disabling of the network controller.
R_NETWORK_TR_CTRL	A 32-bit wide write only register for controlling the Ethernet transmitter.
R_NETWORK_MGM_CTRL	A 32-bit wide write only register for controlling the management interface.
R_NETWORK_STAT	A 32-bit wide read only register for receiver pin status, transmitter error status, and management data.
R_REC_COUNTERS	A 32-bit wide read only register containing receiver error counters.
R_TR_COUNTERS	A 32-bit wide read only register containing transmitter error counters.
R_PHY_COUNTERS	A 32-bit wide read only register containing sqe_test_error and carrier_loss counters.

Table 9-2 Network interface registers

9.3 Network Interface Configuration

The network interface for the ETRAX 100LX is configured in the registers R_NETWORK_REC_CONFIG and R_NETWORK_GEN_CONFIG. In R_NETWORK_GEN_CONFIG, the following configuration possibilities are available:

- Enable/disable the network interface
- Physical interface mode, IEEE 802.3 MII or DP 8391 compatible SNI (see 9.4)
- Frame type and access protocol mode (see 9.6.2 and 9.6.3)

By setting the loopback field of R_NETWORK_GEN_CONFIG, the network interface can also be set in an internal loopback mode where the transmit data is fed directly to the receiver. The data speed in this mode is 100 Mbps.

The R_NETWORK_REC_CONFIG register contains receiver specific configurations (see 9.5). This register also contains the duplex field, which selects between half and full duplex operation.

In full duplex mode, the receiver is not turned off during transmission, and the transmitter ignores the COL and CRS signals. Full duplex flow control is also turned on. This enables the network transmitter of the ETRAX 100LX to automatically react on 802.3x PAUSE frames by temporarily stopping the transmission.

The full duplex mode can also be used for external loopback tests.

Note 1: Unless the transceiver has successfully negotiated full duplex, half duplex should be selected.

9.4 Pin Usage in MII and SNI Modes

Solder Ball	Direction	Name	MII Usage	SNI Usage
Y11	in/out	mdio	Management data.	General I/O.
W11	out	mdc	Management clock.	General output.
V11	out	txdata0	Data out, bit 0.	Data out.
U11	out	txdata1	Data out, bit 1.	General output.
Y12	out	txdata2	Data out, bit 2.	General output.
W12	out	txdata3	Data out, bit 3.	General output.
V12	out	txen	Transmit enable.	Transmit enable.
U12	out	txer	Transmit error/ 25 MHz clock/ Address recognized.	General output.
Y13	in	crs	Carrier sense.	Carrier sense.
W13	in	col	Collision.	Collision.
V13	in	txclk	Transmit clock.	Transmit clock.
Y14	in	rxer	Receive error.	General input.
W14	in	rxclk	Receive clock.	Receive clock.
Y15	in	rxdv	Data in valid.	Not used.
V14	in	rxdata0	Data in, bit 0.	Data in.
W15	in	rxdata1	Data in, bit 1.	General input.
Y16	in	rxdata2	Data in, bit 2.	General input.
U14	in	rxdata3	Data in, bit 3.	General input.

9.5 Receiver Logic Functions

The receiver logic of the ETRAX 100LX network interface, configured in R_NETWORK_REC_CONFIG, performs the following:

- Communicates incoming data to the receiving FIFO of DMA channel 1
- Communicates status to DMA channel 1
- Checks the destination address of the incoming frame
- Checks the CRC of the incoming frame
- Checks the length of the incoming frame

For more information regarding DMA, please refer to chapter *7 DMA*.

9.5.1 Data Transfer to the Receiving FIFO

Incoming data is transferred, one byte at a time, to the receiving FIFO of DMA channel 1. If the destination address of the frame does not match the address in the network interface, or if there is an error in the frame, the frame is aborted and the remaining bytes in the frame are not sent to the FIFO. If an overrun occurs, the packet that caused the overrun is aborted, and reception continues with the next packet.

The frame sent to the FIFO contains the following information:

DA	Destination address (6 bytes)
SA	Source address (6 bytes)
L	Length or type (2 bytes)
Data	Frame data (+ pad if necessary) (46 to 1500 bytes)
CRC	Cyclic Redundancy Check (4 bytes)

The preamble and SOF fields are generated by the PHY/controller.

9.5.2 Address Recognition

The destination address (DA) field of the incoming frame is compared with the addresses set in the network interface. If the addresses do not match, the frame is aborted. Within the frame formats of the IEEE 802.3 standard, there are three types of destination addresses:

- Individual address (unicast)
- Group address (multicast)
- Broadcast (all nodes)

Individual address

The ETRAX 100LX can hold two individual addresses, MA0 and MA1, each 48 bits long. All 48 bits are compared in each address. This means that one or both of the individual addresses can be used to match a group address instead.

In R_NETWORK_REC_CONFIG, there is also one mode bit, ma0 and ma1 respectively, for each individual address to enable/disable recognition.

Group address

A 6-bit hash address is calculated from the 48 destination address (DA) bits:

Hash_address[5:0] =

DA[5:0] ^ DA[11:6] ^ DA[17:12] ^ DA[23:18] ^ DA[29:24] ^ DA[35:30] ^ DA[41:36] ^ DA[47:42]

Note 2: ^ = XOR

The hash address is used as an index for a 64-bit table (R_NETWORK_GA_0 and R_NETWORK_GA_1), which indicates whether or not to copy the frame. In R_NETWORK_REC_CONFIG, there is also the individual mode bit, which is used to select whether to only match group addresses (DA[47] == 1) or to also match individual addresses.

The different addresses above can also be used to get promiscuous mode. Set all bits in R_NETWORK_GA_0 and R_NETWORK_GA_1 to 1, and set the individual field of R_NETWORK_REC_CONFIG to receive (1).

Broadcast address

In R_NETWORK_REC_CONFIG, there is a mode bit broadcast to enable/disable the recognition of the broadcast address 0xFFFFFFFFFFFF.

9.5.3 Receiver CRC Check.

The incoming data is CRC checked according to the IEEE 802.3 standard. If an incorrect CRC is detected, the frame is aborted, and the CRC error counter crc_error or alignment error counter alignment_error is incremented in the register R_REC_COUNTERS. For the difference between these two error counters, please refer to the IEEE 802.3 standard.

With an MII interface, the CRC block also monitors the rxer input signal. If the rxer signal occurs during a reception, this is handled as if an incorrect CRC occurred.

The mode bit bad_crc in R_NETWORK_REC_CONFIG, enables/disables the abortion of frames due to incorrect CRC. If disabled, frames with CRC and alignment errors will also be received. Two status bits, crc_err and align_err, are transferred to DMA channel 1. DMA will put this status information in the status field of the DMA descriptor for the received frame.

9.5.4 Received Frame Length Check

The lengths of the incoming frames are checked against the specified limits of the IEEE 802.3 frame format:

- Minimum: 64 bytes
- Maximum: 1518 or 1522 bytes

The max length of a standard Ethernet packet is 1518 bytes. The length can be extended to 1522 bytes when VLAN tagging, according to IEEE 802.1q, is used. The max length is configured with the max_size field in R_NETWORK_REC_CONFIG.

If the frame length is outside the specified bounds, the frame is aborted. There are two mode bits oversize and undersize in R_NETWORK_REC_CONFIG to enable the minimum length and maximum length check separately.

9.6 Transmitter Logic Functions

The transmitter logic block, configured in R_NETWORK_TR_CTRL, performs the following functions:

- Adds preamble and start of frame delimiter to the beginning of the frame.
- Pads frame data with zeros if the length of the frame data falls below the required minimum of 46 bytes.
- Calculates and adds CRC to the end of the frame.
- Handles the access protocol including automatic retransmission (CSMA/CD or demand priority).

9.6.1 Transmission of Frames

Transmit data is read from the FIFO of DMA channel 0, one byte at a time. The frame from the FIFO should contain the following:

DA	Destination address (6 bytes)
SA	Source address (6 bytes)
L	Length or type (2 bytes)
Data	Frame data (0 to 1500 bytes) (Note 3)

Note 3: Minimum length of data is 46 bytes if automatic pad is not selected.

The transmitter adds the preamble and start-of-frame delimiter to the beginning of the frame, and the frame check sequence (CRC) to the end of the frame. There is an option to automatically add a pad before the CRC, if the data field of the frame is shorter than 46 bytes. The pad consists of all zeros. Automatic padding is selected by the pad bit in R_NETWORK_TR_CTRL.

With the MII interface it is possible to deliberately corrupt a frame by setting the tx_err bit (force network transmission error) in the DMA descriptor. The corruption of frames by the tx_err bit is only possible if the txer pin is configured for transmit error output and is connected to the txer pin of the transceiver.The automatic addition of CRC to the frame can be disabled by setting the crc mode bit in R_NETWORK_TR_CTRL. This allows corrupted frames to be sent, for example, for test purposes.

If the transmitter gets a FIFO empty status during transmission without also getting an eop, the transmission is stopped and the transmit underrun interrupt is activated. The transmitter remains stopped until the interrupt is cleared.

If underrun occurs the transmitter stops. R_DMA_CH0_FIRST points to the first descriptor in the packet that could not be sent.

9.6.2 CSMA/CD Access Protocol

The CSMA/CD access protocol is used in the IEEE 802.3 mode. The protocol listens continuously to carrier sense to see if the line is free. When a frame is queued for transmission, it is sent as soon as the line is free.

If a collision is detected during the transmission, the protocol tries to resend the frame 15 times (i.e. a total of 16 attempts are made). If the transmission is aborted due to excessive collisions, the excessive retry interrupt is issued, and the transmitter stops. The transmitter remains stopped until the interrupt is cleared.

If an excessive collision occurs, the transmitter stops. R_DMA_CH0_FIRST points to the first descriptor in the packet that could not be sent. When the interrupt is cleared, transmission is restarted.

Two mode bits in R_NETWORK_TR_CTRL, retry and cancel, modify the access protocol handling. They can be used for other standard modes, as well as for test purposes or to implement protocols that deviate from the standard.

Field	Description
retry	Retransmission can be disabled. The excessive_col interrupt will then be issued after the first collision.
cancel	A pending frame can be cancelled. This will inhibit any attempts to start sending a frame. If there is data in the FIFO but the transmission has not started, the frame will be aborted. If the transmission is already started it will be completed. No transmit retries will be made if the cancel bit is set. After the current frame is completed or aborted, the excessive_col interrupt will be issued.

9.6.3 Demand Priority Access Protocol

Demand priority access protocol is used in IEEE 802.12 mode. The ETRAX 100LX is designed to support this mode together with Texas Instruments TNETE211 (100-VG-AnyLAN2 PMD interface) or equivalents.

The Ethernet controller also supports the token ring frame format through an 802.3 MII interface with extended protocol, using a handshake protocol. Configuration for this feature is done in R_NETWORK_REC_CONFIG.

For more information about the operation in these modes please contact Axis Communications.

9.7 Management Interface

The MII management interface consists of two pins, mdio and mdc. These pins are controlled by software, and are configured in R_NETWORK_MGM_CTRL.

As an extension of the IEEE 802.3 management protocol, the mdio interrupt is also implemented on the mdio pin. An mdio interrupt will be issued if the mdio field in R_NETWORK_STAT is sampled low while the interrupt is enabled.

In SNI mode, the management interface for the ETRAX 100LX also includes the possibility to use MII_TXD[3:1] and TX_ERR as general outputs, and to use MII_RXD[3:1] and RX_ERR as general inputs.

9.8 Ethernet Error and Statistics Counters

The ETRAX 100LX contains the following Ethernet error and statistics counters which are read in R_REC_COUNTERS, R_TR_COUNTERS and R_PHY_COUNTERS:

Counter	Explanation
crc_error	Number of frames with crc errors
alignment_error	Number of frames with alignment errors
oversize	Number of oversized frames
congestion	Number of otherwise correct frames that were not received due to a FIFO full condition
single_col	Number of frames that were involved in exactly one collision
multiple_col	Number of frames that were involved in more than one collision
late_col	Number of frames that were involved in late collisions
deferred	Number of deferred transmit frames
carrier_loss	Number of transmit frames for which the carrier sense signal was not constantly present during the transmission
sqe_test_error	Number of transmitted frames for which the sqe test signal was not recognized

Each counter is 8 bits wide. The counters are cleared either when they are read or at system reset. When a counter reaches 255 it stops counting. If the network interface is disabled the counter values are preserved.

An interrupt (with the same name as the error counter) is generated for a counter when it reaches 128. Reading the counter will clear the associated interrupt. The interrupt status can be masked individually, but all counters share the same interrupt vector number (0x27).

9.9 Network interrupts

In addition to error and statistics counter interrupts, there are four network interrupts. Two of these interrupts are for the network receiver, one is for the network transmitter, and one is for the mdio pin. All have the internally generated vector number 0x26.

overrun

This interrupt is set when the network receiver experiences a FIFO overrun condition (congestion error). Two interrupts, congestion (See section 9.8) and overrun, are available, but usually only one of them should be enabled. The overrun interrupt should be used if software intervention is necessary when an overrun error occurs. The congestion error counter should be used if the only action needed is an error count.

This interrupt is cleared by reading the congestion field of R_REC_COUNTERS, an action which also clears the congestion interrupt.

underrun

This interrupt is set when the network transmitter experiences a FIFO underrun condition. This interrupt is cleared by setting the clr_error field in R_NETWORK_TR_CTRL.

excessive_col

This interrupt is set when the network transmitter experiences collisions for 16 consecutive transmission attempts. It is set after the first collision if the retry field in network interface register R_NETWORK_TR_CTRL is set to disable, and when the transmitter stops after the cancel field of R_NETWORK_TR_CTRL has been set. This interrupt is cleared by setting the clr_error field in R_NETWORK_TR_CTRL.

mdio

This interrupt is from the MII mdio pin. It is generated when the mdio pin is low. The interrupt should be masked off during normal data transfers over the mdio interface. This interrupt should be cleared in the external unit that is driving the MDIO pin.

For more information see chapter 17 *Interrupts.*