10 EIDE/ATA-2/ATA-3 INTERFACE

10.1 ATA Interface Pin Connection

The EIDE/ATA-2/ATA-3, or ATA interface for short, supports four ATA busses without external logic, see Figure 10-1 below.

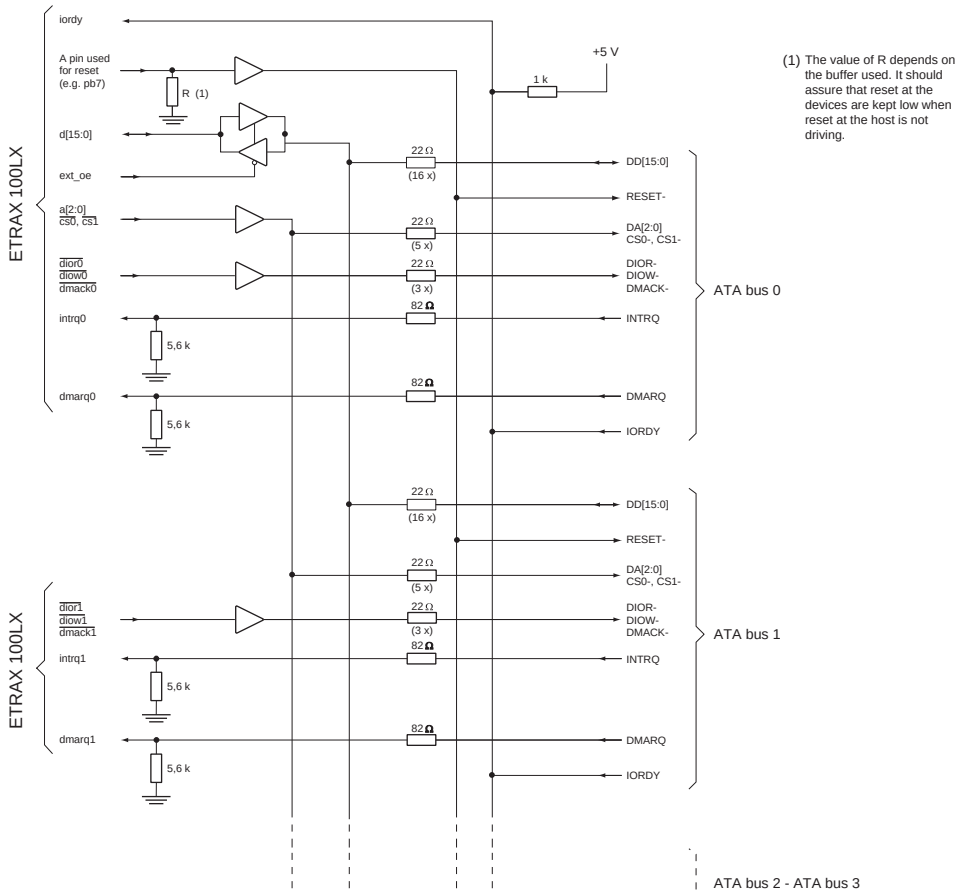

Figure 10-1 How to Connect the ATA Bus.

Each bus is capable of accessing two ATA devices, so up to a total of eight devices can be accessed by the ATA interface.

The ATA interface is enabled in the R_GEN_CONFIG register (See 18.11 *ATA Interface Registers*).

The reset signal of the ATA interface (RESET- (Device reset)) is not supported by the hardware of the ETRAX 100LX, but must be chosen from an available general I/O pin (e.g. General Port pa0 - pa7, General Port pb0 - pb7, g27, etc.) and handled by software. For more information regarding general I/O pins see chapter 19 *Electrical Information*.

10.2 EIDE/ATA-2/ATA-3 Interface Registers

An ATA/ATAPI device (e.g. a hard disk or CD-ROM drive) is controlled via a set of read/write registers in each device. By writing to these registers the ATA device can be made to perform commands such as reading or writing data to or from a disk. For more information about these registers please see the ATA-3 standard.

Communication between the ETRAX 100LX and ATA devices takes place via the following set of ETRAX 100LX registers:

Register	Function
R_ATA_CTRL_DATA	A 32-bit write only register to enable reading data from and writing data to ATA devices.
R_ATA_STATUS_DATA	A 32-bit read only register that indicates if the ATA interface is busy. It also indicates if the transmitter is ready, and holds data read from the ATA device.
R_ATA_CONFIG	A 32-bit write only register for enabling the ATA controller, DMA handshaking, and setup and hold time for register read/writes.
R_ATA_TRANSFER_CNT	A 32-bit read/write register used to set the number of bytes or 16-bit words transferred during DMA transfers.

For more detailed information about these registers, see chapter 18.11 *ATA Interface Registers*

10.3 Data Transfer

The ATA interface of ETRAX 100LX can be driven either by internal DMA or by using the register R_ATA_CTRL_DATA (see sections 10.3.3 ETRAX 100LX Register Access, and 10.3.4 ETRAX 100LX DMA Access below). Programmed input/output (PIO) is used for transferring commands to the ATA device, and for transferring data if the device does not support the DMA handshaking protocol.

Internal DMA of the ETRAX 100LX must not be confused with the DMA handshaking on the ATA bus that many ATA devices use. ETRAX 100LX DMA can be used both when directly accessing the ATA registers of the device Programmed Input/Output (PIO) and when using the DMA handshaking protocol of the device.

10.3.1 Programmed Input/Output (PIO)

Commands are always transferred to ATA devices using PIO, and the commands are written directly to the R_ATA_CTRL_DATA register in the ETRAX 100LX. Data can also be transferred to ATA devices in the same way. Data fetched from ATA devices is read in R_ATA_STATUS_DATA.

10.3.2 ATA DMA Handshaking

Most new ATA devices use DMA handshaking to transfer data. DMA handshaking is enabled in R_ATA_CONFIG.

The device sets its DMARQ signal high when it is ready to receive or deliver data. If the amount to be transferred to or from the device is large, it is possible that the device can neither accept nor produce all data in one burst. It will then lower its

DMARQ for periods of time during the transfer. It may take some time until the device is able to accept or produce more data after it has lowered its DMARQ, so this time can be used to talk to another ATA device. This is made possible through the ata_dmaend interrupt generated when the DMARQ signal goes low.

10.3.3 ETRAX 100LX Register Access

The R_ATA_CTRL_DATA register of the ETRAX 100LX is used for writing to or reading from the registers of ATA devices. Each time R_ATA_CTRL_DATA is written to, one transfer is made to or from the ATA device. The result (e.g. the data transferred from the ATA device) is read in R_ATA_STATUS_DATA.

10.3.4 ETRAX 100LX DMA Access

An alternative to register access is to let internal DMA of the ETRAX 100LX drive the ATA interface, which is then used to transfer data to and from the ATA device. Configuration to allow DMA to drive the ATA interface is done in R_GEN_CONFIG. ATA uses DMA channels 2 and 3.

A transfer counter, R_ATA_TRANSFER_CNT, is used. For each ATA transfer (8 or 16 bits) the counter is decremented. When the R_ATA_TRANSFER_CNT register reaches zero, the transfer is stopped. If data was transferred to the ETRAX 100LX, an end-of-packet (EOP) is signalled to ETRAX 100LX DMA.

10.4 Timing

If PIO is used, the time for transferring individual data varies between 140 ns and 600ns depending on what mode the ATA device is in (For details please see the ATA-3 standard).

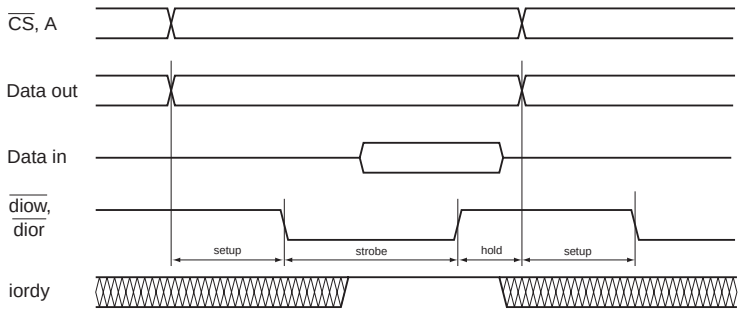

Figure 10-2 PIO Timing

When DMA handshaking is used, the time varies from 120 ns to 480 ns depending on the ATA mode.

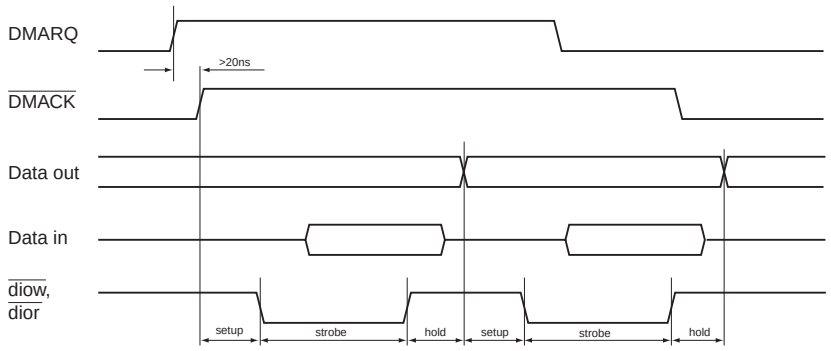

Figure 10-3 DMA Multiword (16-bit) Timing

Timing for both PIO and DMA handshaking is configured in R_ATA_CONFIG.

10.5 Interrupts

The ATA interface has nine interrupts:

ata_irq0, ata_irq1, ata_irq2, and ata_irq3

When ATA is in use, ata_irq0, ata_irq1, ata_irq2, or ata_irq3 is set when a unit on the ATA bus (0, 1, 2, 3 respectively) requests an interrupt. The interrupt is cleared through registers in the external unit on the ATA bus (0, 1, 2, 3 respectively).

ata_drq0, ata_drq1, ata_drq2, and ata_drq3

Whe ATA is in use, ata_drq0, ata_drq1, ata_drq2, or ata_drq3 is set when a unit on the ATA bus (0, 1, 2, 3 respectively) requests a DMA transfer. The interrupt is automatically cleared at the end of the DMA transfer on ATA bus (0, 1, 2, 3 respectively).

ata_dmaend

The ata_dmaend interrupt is set when the selected ATA unit releases its DMA request (transfer completed). The interrupt should be masked in R_IRQ_MASK0_SET except when an ATA DMA transfer has been started. It is automatically cleared when the next ATA DMA transfer commences.