

14 SHARED RAM INTERFACE

The shared RAM interface handles 8-bit and 16-bit transfers between an external device and the system SRAM. The interface operates with standard SRAM. Data transfers are controlled by an asynchronous handshake protocol.

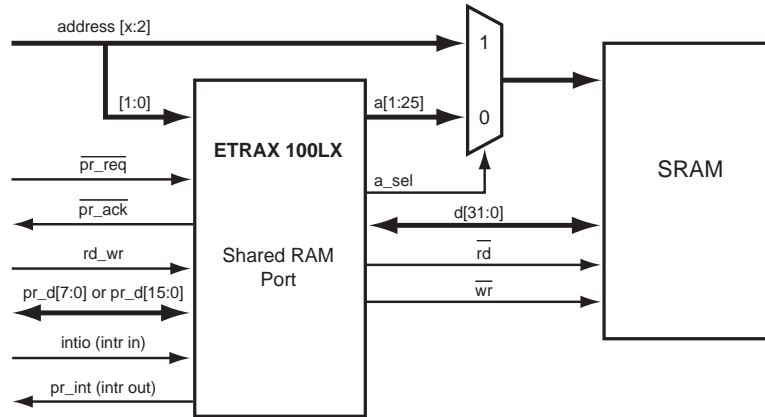


Figure 14-1 How to Connect for Shared RAM

The address from the external device is supplied to the SRAM through external multiplexers, except for address bit 0 and 1 that are multiplexed internally.

Shared RAM interface cycles are like normal bus cycles, except that the **a_sel** signal on the **s0atn** pin is high during the cycle. Shared RAM interface cycles are never packed together in bursts. The cycles can be 8-bit or 16-bit wide. 16-bit cycles are always 16-bit aligned.

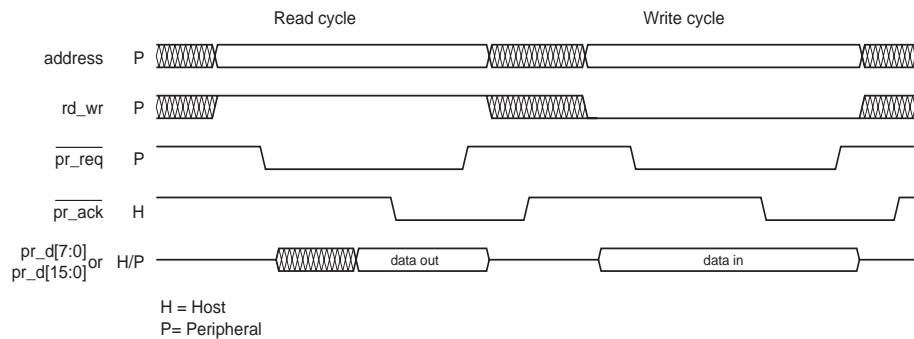


Figure 14-2 Shared RAM Timing

14.1 Shared RAM Interface Configuration

Register	Function
R_SHARED_RAM_CONFIG	A 32-bit write only register to configure and enable the shared RAM interface.
R_SHARED_RAM_ADDR	A 32-bit write only register that sets bits 29-8 of the base address for the shared RAM area.

Table 14-1 Shared RAM Interface Registers

To initiate the Shared RAM interface, first write to the R_GEN_CONFIG register, then to R_SHARED_RAM_ADDR, and finally to R_SHARED_RAM_CONFIG. For more information see chapter 18.5 *Shared RAM Interface Registers*.

14.2 Shared RAM Interrupts

One interrupt signal in each direction is provided. The incoming interrupt set on the Shared RAM interface **intio** pin is negative edge triggered. The interrupt is cleared by setting the **clri** bit of the R_SHARED_RAM_CONFIG register.

The interrupt going out, set on the Shared RAM interface pin **pr_int**, is active low and stays low for 600 ns. This interrupt is generated if the **pint** field in R_SHARED_RAM_CONFIG is set to **int**.