

19 Electrical Information

19.1 Pinout

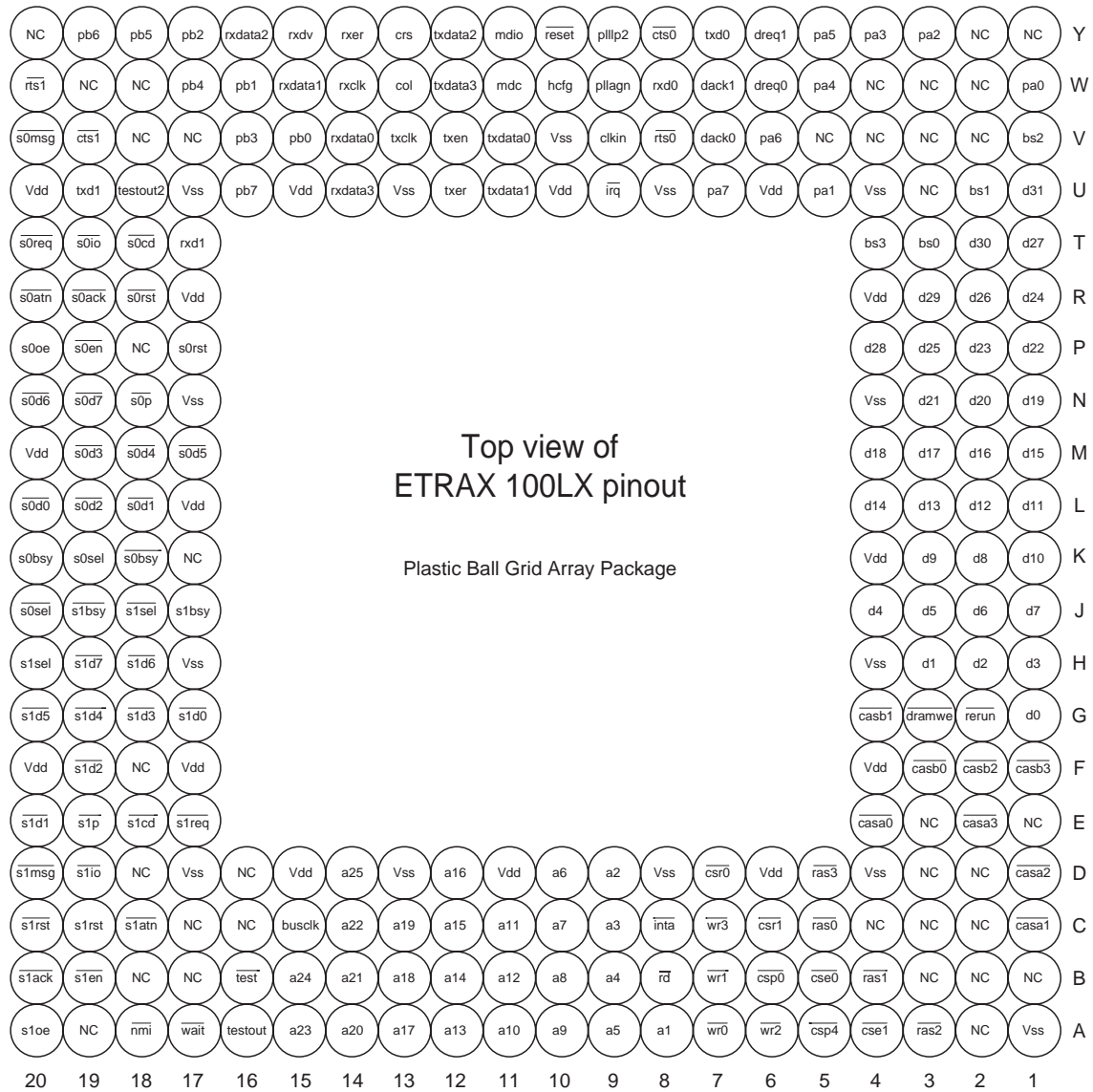


Figure 19-1 The ETRAX 100LX Pinout

19.2 Clock and PLL Signals

Solder Ball	Name	Direction	Description
V9	clkin	in	External clock input.
W9	pllagn	out	PLL loop filter internal ground connection.
Y9	pllp2	in/out	PLL loop filter.

Table 19-1 Clock and Phase-locked Loop Signals

19.3 Power and Ground Signals

Solder Ball	Name	Description
A1 D4 D8 D13 D17 H4 H17 N4 N17 U4 U8 U13 U17 V10	V _{ss}	Ground connection.
D6 D11 D15 F4 F17 F20 K4 L17 M20 R4 R17 U6 U10 U15 U20	V _{dd}	Supply voltage, 3.3 V.

Table 19-2 Power and Ground Signals

19.4 Bus Interface Signals

Data Bus

Solder Ball	Direction	Pin Name
G1	in/out	d0
H3	in/out	d1
H2	in/out	d2
H1	in/out	d3
J4	in/out	d4
J3	in/out	d5
J2	in/out	d6
J1	in/out	d7
K2	in/out	d8
K3	in/out	d9
K1	in/out	d10
L1	in/out	d11
L2	in/out	d12
L3	in/out	d13
L4	in/out	d14
M1	in/out	d15
M2	in/out	d16
M3	in/out	d17
M4	in/out	d18
N1	in/out	d19
N2	in/out	d20
N3	in/out	d21
P1	in/out	d22
P2	in/out	d23
R1	in/out	d24
P3	in/out	d25
R2	in/out	d26
T1	in/out	d27
P4	in/out	d28
R3	in/out	d29
T2	in/out	d30
U1	in/out	d31

Address Bus

Solder Ball	Direction	Pin Name
A8	out	a1 (Note 1)
D9	out	a2
C9	out	a3
B9	out	a4
A9	out	a5
D10	out	a6
C10	out	a7
B10	out	a8
A10	out	a9
A11	out	a10
C11	out	a11
B11	out	a12
A12	out	a13
B12	out	a14
C12	out	a15
D12	out	a16
A13	out	a17
B13	out	a18
C13	out	a19
A14	out	a20
B14	out	a21
C14	out	a22
A15	out	a23 (Note 2)
B15	out	a24 (Note 2)
D14	out	a25 (Note 2)

Table 19-3 Data and Address Buses

Note 1: Solder ball A8 is dual-function. See table 19-5.

Note 2: Solder balls A15, B15 and D14 are dual-function. See table 19-6.

Chip Select Signals

Solder Ball	Direction	Pin Name	Description
B5	out	$\overline{\text{cse0}}$	Chip select signal for EPROM/flashPROM 0.
A4	out	$\overline{\text{cse1}}$	Chip select signal for EPROM/flashPROM 1.
D7	out	$\overline{\text{csr0}}$	Chip select signal for SRAM 0.
C6	out	$\overline{\text{csr1}}$	Chip select signal for SRAM 1.
B6	out	$\overline{\text{csp0}}$	Peripheral chip select signal 0.
A5	out	$\overline{\text{csp4}}$	Peripheral chip select signal 4.

Table 19-4 Chip Select Signals

Peripheral chip select signals $\overline{\text{csp1}}$ to $\overline{\text{csp3}}$ and $\overline{\text{csp5}}$ to $\overline{\text{csp7}}$ are multiplexed with bits pb2 to pb7 in general port PB. See tables 19-19 and 19-20.

Read/Write Strobes

Solder Ball	Direction	Bytewise Write Enable	Common Write Enable		Description
			16-bit Mode	32-bit Mode	
B8	out	$\overline{\text{rd}}$	$\overline{\text{rd}}$	$\overline{\text{rd}}$	Read strobe, common to all four bytes of the data bus. Not active during DRAM access.
A7	out	$\overline{\text{wr0}}$			Write strobe for byte 0 of the data bus.
			$\overline{\text{be0}}$	$\overline{\text{be0}}$	Byte enable strobe for byte 0 of the data bus.
B7	out	$\overline{\text{wr1}}$			Write strobe for byte 1 of the data bus.
			$\overline{\text{be1}}$	$\overline{\text{be1}}$	Byte enable strobe for byte 1 of the data bus.
A6	out	$\overline{\text{wr2}}$			Write strobe for byte 2 of the data bus.
				$\overline{\text{be2}}$	Byte enable strobe for byte 2 of the data bus.
C7	out	$\overline{\text{wr3}}$			Write strobe for byte 3 of the data bus.
			$\overline{\text{we}}$	$\overline{\text{we}}$	Write enable strobe, common to all four bytes of the data bus.
A8	out	a1	a1		Least significant address bit.
				$\overline{\text{be3}}$	Byte enable strobe for byte 3 of the data bus.

Table 19-5 Read/Write Strobe Signals for Bytewise and Common Write Enable Modes

Asynchronous and Synchronous DRAM Signals

Solder Ball	Direction	Asynchronous DRAM		Sync. DRAM	Description
		Byte-wise Mode	Bank-wise Mode		
E4	out	$\overline{\text{casa0}}$			Column address strobe for byte 0 in Async. DRAM bank 0 and 1.
			$\overline{\text{casa0}}$		Column address strobe for Async. DRAM bank 0.
				dqm0	Data qualify mask 0.
C1	out	$\overline{\text{casa1}}$			Column address strobe for byte 1 in Async. DRAM bank 0 and 1.
			$\overline{\text{casa1}}$		Column address strobe for Async. DRAM bank 1.
				dqm1	Data qualify mask 1.
D1	out	$\overline{\text{casa2}}$			Column address strobe for byte 2 in Async. DRAM bank 0 and 1.
			$\overline{\text{casa2}}$		Column address strobe for Async. DRAM bank 2.
				dqm2	Data qualify mask 2.
E2	out	$\overline{\text{casa3}}$			Column address strobe for byte 3 in Async. DRAM bank 0 and 1.
			$\overline{\text{casa3}}$		Column address strobe for Async. DRAM bank 3.
				dqm3	Data qualify mask 3.
F3	out	$\overline{\text{casb0}}$			Column address strobe for byte 0 in Async. DRAM bank 2 and 3.
			$\overline{\text{be0}}$		Enable signal for byte 0 of the data bus.
				dqm4	Data qualify mask 4.
G4	out	$\overline{\text{casb1}}$			Column address strobe for byte 1 in Async. DRAM bank 2 and 3.
			$\overline{\text{be1}}$		Enable signal for byte 1 of the data bus.
				dqm5	Data qualify mask 5.
F2	out	$\overline{\text{casb2}}$			Column address strobe for byte 2 in Async. DRAM bank 2 and 3.
			$\overline{\text{be2}}$		Enable signal for byte 2 of the data bus.
				dqm6	Data qualify mask 6.
F1	out	$\overline{\text{casb3}}$			Column address strobe for byte 3 in Async. DRAM bank 2 and 3.
			$\overline{\text{be3}}$		Enable signal for byte 2 of the data bus.
				dqm7	Data qualify mask 7.
G3	out	$\overline{\text{dramwe}}$	$\overline{\text{dramwe}}$		Write enable signal for Async. DRAM.
	in/out			dqs	DDR data qualify strobe.
C5	out	$\overline{\text{ras0}}$	$\overline{\text{ras0}}$		Row address strobe for Async. DRAM bank 0.
				$\overline{\text{csd0}}$	Chip select signal for Sync. DRAM group 0.
B4	out	$\overline{\text{ras1}}$	$\overline{\text{ras1}}$		Row address strobe for Async. DRAM bank 1.
				$\overline{\text{csd1}}$	Chip select signal for Sync. DRAM group 1.
A3	out	$\overline{\text{ras2}}$	$\overline{\text{ras2}}$		Row address strobe for Async. DRAM bank 2.
				clk	Master clock signal for Sync. DRAM.
D5	out	$\overline{\text{ras3}}$	$\overline{\text{ras3}}$		Row address strobe for Async. DRAM bank 3.
				cke	Clock enable for Sync. DRAM.
A15	out	a23	a23		Bit 23 of address bus.
				$\overline{\text{sdr_we}}$	Write enable signal for Sync. DRAM.
B15	out	a24	a24		Bit 24 of address bus.
				$\overline{\text{sdr_cas}}$	Column address strobe for Sync. DRAM.
D14	out	a25	a25		Bit 25 of address bus.
				$\overline{\text{sdr_ras}}$	Row address strobe for Sync. DRAM.

Table 19-6 Asynchronous and Synchronous DRAM Signals

Miscellaneous Bus Interface Signals

Solder Ball	Direction	Name	Description
G2	in	$\overline{\text{rerun}}$	Bus rerun signal.
W6	in	dreq0	DMA request, external DMA0.
Y6	in	dreq1	DMA request, external DMA1.
V7	out	dack0	DMA acknowledge, external DMA0.
W7	out	dack1	DMA acknowledge, external DMA1.
U9	in	$\overline{\text{irq}}$	Interrupt request.
A18	in	$\overline{\text{nmi}}$	Non maskable interrupt request.
A17	in	$\overline{\text{wait}}$	External wait state input.
C8	out	$\overline{\text{inta}}$	External interrupt acknowledge.
Y10	in	$\overline{\text{reset}}$	System reset.
W10	in	hcfg	Hardware configuration for serial ports 2 and 3.

Table 19-7 Miscellaneous Bus Interface Signals

19.5 Logic Analyzer Mode and Test Signals

Solder Ball	Direction	Name	Description
T3	in/out	bs0	Bus status, bit 0 (Note 3).
U2	in/out	bs1	Bus status, bit 1 (Note 3).
V1	in/out	bs2	Bus status, bit 2 (Note 3).
T4	in/out	bs3	Bus status, bit 3 (Note 3).
B16	in	$\overline{\text{test}}$	Test input, should be high for normal operation.
A16	out	testout	Test output, must not be connected.
C15	out	busclk	Bus synchronization clock. Used for debug purposes.
U18	out	testout2	Test output, must not be connected.

Table 19-8 Logic Analyzer Mode and Test Signals

Note 3: These signals are for bus configuration during power-on reset. They are used as status outputs for debugging purposes when reset is inactive.

19.6 General Port PA Signals

Solder Ball	Direction	Name	Description
W1	in/out	pa0	General port PA, bit 0.
U5	in/out	pa1	General port PA, bit 1.
Y3	in/out	pa2	General port PA, bit 2.
Y4	in/out	pa3	General port PA, bit 3.
W5	in/out	pa4	General port PA, bit 4.
Y5	in/out	pa5	General port PA, bit 5.
V6	in/out	pa6	General port PA, bit 6.
U7	in/out	pa7	General port PA, bit 7.

Table 19-9 General Port PA Signals

19.7 Asynchronous Serial Port 0 Signals

Solder Ball	Direction	Name	Description
Y7	out	txd0	Transmit data, serial port 0.
V8	out	$\overline{\text{rts0}}$	Request to send, serial port 0.
W8	in	rxd0	Receive data, serial port 0.
Y8	in	$\overline{\text{cts0}}$	Clear to send, serial port 0.

Table 19-10 Serial Port 0 Signals

Note 4: I/O signals at Asynchronous Serial Ports p1 to p3 are multiplexed on to pins used by other interfaces. Sections 19-9 and 19-10 refer.

19.8 Network Interface Signals

Solder Ball	Direction	Name	MII Usage	SNI Usage
Y11	in/out	mdio	Management data.	General I/O.
W11	out	mdc	Management clock.	General output.
V11	out	txdata0	Data out, bit 0.	Data out.
U11	out	txdata1	Data out, bit 1.	General output.
Y12	out	txdata2	Data out, bit 2.	General output.
W12	out	txdata3	Data out, bit 3.	General output.
V12	out	txen	Transmit enable.	Transmit enable.
U12	out	txer	Transmit error/ 25 MHz clock/ Address recognized.	General output.
Y13	in	crs	Carrier sense.	Carrier sense.
W13	in	col	Collision.	Collision.
V13	in	txclk	Transmit clock.	Transmit clock.
Y14	in	rxer	Receive error.	General input.
W14	in	rxclk	Receive clock.	Receive clock.
Y15	in	rxdv	Data in valid.	Not used.
V14	in	rxdata0	Data in, bit 0.	Data in.
W15	in	rxdata1	Data in, bit 1.	General input.
Y16	in	rxdata2	Data in, bit 2.	General input.
U14	in	rxdata3	Data in, bit 3.	General input.

Table 19-11 Network Interface Signals

19.9 Multiplexed Signal Groups

To optimize chip efficiency and minimize the device footprint, certain interfaces share a number of I/O pins. The input and outputs to and from these interfaces are multiplexed on to these common pins. The table below lists the interfaces whose inputs and outputs are multiplexed in this way.

Interface
Asynchronous Serial Port p1
Asynchronous Serial Port p2
Asynchronous Serial Port p3
Synchronous Serial Port p1
Synchronous Serial Port p3
Shared RAM (8-bit)
Shared RAM-W (16-bit wide)
Parallel Port p0
Parallel Port p1
Parallel Port-W (16-bit wide)
SCSI-8 Port p0
SCSI-8 Port p1
SCSI-W (16-bit wide)
ATA interface
Additional Chip Select (CSP)
I2C Port
USB interface port p1
USB interface port p2
General I/O pins

Table 19-12 Multiplexed Interfaces

The I/O pins on to which the interface signals are multiplexed are arranged in six groups denoted A to F respectively. The table on the next page maps the relationships between the groups of pins and the interfaces that use them. It shows that some interfaces are mutually exclusive - they cannot use the I/O pins simultaneously. For example it is not possible to use SCSI-8 p0 at the same time as Asynchronous Serial Port p2 because the four Group B pins used by the serial port are also required for the SCSI interface.

Pins that are not used by a particular interface are available for general I/O purposes.

I/O PIN GROUPS					
A (19 pins)	B (4 pins)	C (4 pins)	D (19 pins)	E (4 pins)	F (8 pins)
–	Asynchronous Serial Port p2	Asynchronous Serial Port p3	–	Asynchronous Serial Port p1	–
–	–	Synchronous Serial Port p3	–	Synchronous Serial Port p1	Synchronous Serial Port p1 (Note 5)
–	–	–	–	–	Synchronous Serial Port p3 (Note 5)
Shared RAM	–	–	–	–	–
Shared RAM-W	–	–	Shared RAM-W	–	–
Parallel Port p0	–	–	Parallel Port p1	–	–
Parallel Port-W	–	–	Parallel Port-W	–	–
SCSI-8 Port p0	SCSI-8 Port p0	–	–	–	SCSI-8 Port p0 (Note 5)
–	–	SCSI-8 Port p1	SCSI-8 Port p1	–	SCSI-8 Port p1 (Note 5)
SCSI-W Port	SCSI-W Port	–	SCSI-W Port	–	SCSI-W Port
ATA Port	ATA Port	ATA Port	ATA Port	–	–
–	–	–	–	–	CSP and I2C Port
–	–	–	USB Port p2	USB Port p1	USB Port p1
General I/O Port	General I/O Port	General I/O Port	General I/O Port	General I/O Port	General I/O Port

Table 19-13 Multiplexed Interfaces and I/O Pin Groups

Note 5: These ports use only two pins of I/O pin Group F. Consequently the two synchronous serial ports are not mutually exclusive of each other because unused pins remain available. Similarly the two SCSI-8 ports are not mutually exclusive of each other. However the *pairs of ports* are mutually exclusive because, in Group F, Synchronous Serial Port p1 and SCSI-8 p0 both use pin W17, and Synchronous Serial Port p3 and SCSI-8 p1 both use pin U16.

19.9.1 Multiplexed I/O Signals - Group A

INTERFACES																
Pin	SCSI-8 p0		SCSI-W		ATA		Parallel Port p0		Parallel Port-W		Shared RAM/ Shared RAM-W		General I/O			
V20	s0msg	in/out	s0msg	in/out	iordy	in	p0perror	in	p0perror	in	pr_adr0	in	-	-	g5	in
T18	s0cd	in/out	s0cd	in/out	dmarq0	in	p0ack	in	p0ack	in	pr_adr1	in	-	-	g4	in
T19	s0io	in/out	s0io	in/out	dmarq1	in	p0busy	in	p0busy	in	intio	in	-	-	g3	in
T20	s0req	in	s0req	in	dmarq2	in	p0fault	in	p0fault	in	rd_wr	in	-	-	g2	in
R18	s0rst	in	s0rst	in	dmarq3	in	p0select	in	p0select	in	pr_req	in	-	-	g1	in
P17	s0rst	out	s0rst	out	cs0	out	p0data_oe	out	p0data_oe	out	pr_int	out	-	-	g5	out
R19	s0ack	out	s0ack	out	cs1	out	p0selectin	out	p0selectin	out	pr_ack	out	-	-	g4	out
R20	s0atn	out	s0atn	out	a0	out	p0autofd	out	p0autofd	out	a_sel	out	-	-	g3	out
K20	s0bsy	out	s0bsy	out	a1	out	p0strobe	out	p0strobe	out	-	-	-	-	g2	out
P20	s0oe	out	s0oe	out	a2	out	p0init	out	p0init	out	-	-	-	-	g1	out
N18	s0p	in/out	s0p	in/out	dmack0	out	-	-	-	-	-	-	-	-	g0	in/out
N19	s0d7	in/out	s0d7	in/out	d7	in/out	p0d7	in/out	p0d7	in/out	pr_d7	in/out	-	-	g15	in/out
N20	s0d6	in/out	s0d6	in/out	d6	in/out	p0d6	in/out	p0d6	in/out	pr_d6	in/out	-	-	g14	in/out
M17	s0d5	in/out	s0d5	in/out	d5	in/out	p0d5	in/out	p0d5	in/out	pr_d5	in/out	-	-	g13	in/out
M18	s0d4	in/out	s0d4	in/out	d4	in/out	p0d4	in/out	p0d4	in/out	pr_d4	in/out	-	-	g12	in/out
M19	s0d3	in/out	s0d3	in/out	d3	in/out	p0d3	in/out	p0d3	in/out	pr_d3	in/out	-	-	g11	in/out
L19	s0d2	in/out	s0d2	in/out	d2	in/out	p0d2	in/out	p0d2	in/out	pr_d2	in/out	-	-	g10	in/out
L18	s0d1	in/out	s0d1	in/out	d1	in/out	p0d1	in/out	p0d1	in/out	pr_d1	in/out	-	-	g9	in/out
L20	s0d0	in/out	s0d0	in/out	d0	in/out	p0d0	in/out	p0d0	in/out	pr_d0	in/out	-	-	g8	in/out

Table 19-14 Multiplexed I/O Signals - Group A

19.9.2 Multiplexed I/O Signals - Group B

INTERFACES																
Pin	SCSI-8 p0		SCSI-W		ATA		Async. Serial Port p2						General I/O			
P19	s0en	out	s0en	out	dior0	out	rts2	out	-	-	-	-	-	-	g7	out
K19	s0sel	out	s0sel	out	dior1	out	txd2	out	-	-	-	-	-	-	g6	out
K18	s0bsy	in	s0bsy	in	intrq0	in	cts2	in	-	-	-	-	-	-	g7	in
J20	s0sel	in	s0sel	in	intrq1	in	rxid2	in	-	-	-	-	-	-	g6	in

Table 19-15 Multiplexed I/O Signals - Group B

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19.9.3 Multiplexed I/O Signals - Group C

INTERFACES														
Pin	SCSI-8 p1		ATA		Async. Serial Port p3		Sync. Serial Port p3					General I/O		
J19	$\overline{s1bsy}$	in	-	-	intrq2	in	$\overline{cts3}$	in	ss3_in2	in	-	-	g31	in
J18	$\overline{s1sel}$	in	-	-	intrq3	in	rx3	in	ss3_in1	in	-	-	g30	in
B19	$\overline{s1en}$	out	-	-	$\overline{dior2}$	out	$\overline{rts3}$	out	ss3_out2	out	-	-	g31	out
H20	s1sel	out	-	-	$\overline{dior3}$	out	tx3	out	ss3_out1	out	-	-	g30	out

Table 19-16 Multiplexed I/O Signals - Group C

19.9.4 Multiplexed I/O Signals - Group D

INTERFACES																
Pin	SCSI-8 p1		SCSI-W		ATA		Parallel Port p1		Parallel Port-W		Shared RAM-W		USB Port p2		General I/O	
H19	$\overline{s1d7}$	in/out	$\overline{s0d15}$	in/out	d15	in/out	p1d7	in/out	p0d15	in/out	pr_d15	in/out	-	-	g23	in/out
H18	$\overline{s1d6}$	in/out	$\overline{s0d14}$	in/out	d14	in/out	p1d6	in/out	p0d14	in/out	pr_d14	in/out	-	-	g22	in/out
G20	$\overline{s1d5}$	in/out	$\overline{s0d13}$	in/out	d13	in/out	p1d5	in/out	p0d13	in/out	pr_d13	in/out	-	-	g21	in/out
G19	$\overline{s1d4}$	in/out	$\overline{s0d12}$	in/out	d12	in/out	p1d4	in/out	p0d12	in/out	pr_d12	in/out	-	-	g20	in/out
G18	$\overline{s1d3}$	in/out	$\overline{s0d11}$	in/out	d11	in/out	p1d3	in/out	p0d11	in/out	pr_d11	in/out	-	-	g19	in/out
F19	$\overline{s1d2}$	in/out	$\overline{s0d10}$	in/out	d10	in/out	p1d2	in/out	p0d10	in/out	pr_d10	in/out	-	-	g18	in/out
E20	$\overline{s1d1}$	in/out	$\overline{s0d9}$	in/out	d9	in/out	p1d1	in/out	p0d9	in/out	pr_d9	in/out	-	-	g17	in/out
G17	$\overline{s1d0}$	in/out	$\overline{s0d8}$	in/out	d8	in/out	p1d0	in/out	p0d8	in/out	pr_d8	in/out	-	-	g16	in/out
E19	$\overline{s1p}$	in/out	$\overline{s0p1}$	in/out	$\overline{dmack1}$	out	-	-	-	-	-	-	-	-	g24	in/out
D20	$\overline{s1msg}$	in/out	-	-	$\overline{dmack2}$	out	p1perror	in	-	-	-	-	$\overline{usb2_oe}$	out	g29	in
E18	$\overline{s1cd}$	in/out	-	-	$\overline{dmack3}$	out	\overline{plack}	in	-	-	-	-	usb2_speed	out	g28	in
D19	$\overline{s1io}$	in/out	-	-	g27	out	p1busy	in	-	-	-	-	usb2_rcv	in	g27	in
E17	$\overline{s1req}$	in	-	-	-	-	$\overline{p1faul}$	in	-	-	-	-	usb2_vp	in	g26	in
C20	$\overline{s1rst}$	in	-	-	-	-	p1select	in	-	-	-	-	usb2_vm	in	g25	in
C19	s1rst	out	-	-	$\overline{diow0}$	out	p1data_oe	out	-	-	-	-	-	-	g29	out
B20	$\overline{s1ack}$	out	-	-	$\overline{diow1}$	out	$\overline{p1selectin}$	out	-	-	-	-	-	-	g28	out
C18	$\overline{s1atn}$	out	-	-	$\overline{diow2}$	out	$\overline{p1autofd}$	out	-	-	-	-	usb2_vpo	out	g27	out
J17	s1bsy	out	$\overline{s0enhiid}$	out	$\overline{diow3}$	out	$\overline{p1strobe}$	out	-	-	-	-	usb2_vmo	out	g26	out
A20	s1oe	out	s1oe	out	ext_oe	out	$\overline{p1imit}$	out	-	-	-	-	-	-	g25	out

Table 19-17 Multiplexed I/O Signals - Group D

19.9.5 Multiplexed I/O Signals - Group E

INTERFACES												
Pin					Sync. Serial Port p1	Async. Serial Port p1					USB Port p1	
U19	-	-	-	-	ss1_out1 out	txd1 out	-	-	-	-	$\overline{\text{usb1_oe}}$ out	
W20	-	-	-	-	ss1_out2 out	$\overline{\text{rts1}}$ out	-	-	-	-	usb1_speed out	
T17	-	-	-	-	ss1_in1 in	rxd1 in	-	-	-	-	usb1_rcv in	
V19	-	-	-	-	ss1_in2 in	$\overline{\text{cts1}}$ in	-	-	-	-	usb1_vp in	

Table 19-18 Multiplexed I/O Signals - Group E

19.9.6 Multiplexed I/O Signals - Group F

INTERFACES												
Pin	SCSI-8 p0		SCSI-8 p1		SCSI-W		Sync. Serial Port p1	Sync. Serial Port p3	CSP and I2C		USB Port p1	General I/O
V15	-	-	-	-	-	-	-	-	i2c_d in/out	-	-	pb0 in/out
W16	-	-	-	-	-	-	-	-	i2c_clk out	-	-	pb1 in/out
Y17	-	-	-	-	-	-	-	-	$\overline{\text{csp1}}$ out	usb1_vpo out	-	pb2 in/out
V16	-	-	-	-	-	-	-	-	$\overline{\text{csp2}}$ out	usb1_vmo out	-	pb3 in/out
W17	$\overline{\text{s0enph}}$ out	-	-	-	$\overline{\text{s0enph}}$ out	-	ss1_io3 in/out	-	-	$\overline{\text{csp3}}$ out	-	pb4 in/out
Y18	-	-	-	-	-	-	-	-	$\overline{\text{csp5}}$ out	usb1_vm in	-	pb5 in/out
Y19	-	-	-	-	-	-	-	-	$\overline{\text{csp6}}$ out	-	-	pb6 in/out
U16	-	-	$\overline{\text{s1enph}}$ out	s0enloid out	-	-	ss3_io3 in/out	-	$\overline{\text{csp7}}$ out	-	-	pb7 in/out

Table 19-19 Multiplexed I/O Signals - Group F

19.10 Multiplexed Interfaces

This section provides signal assignment details of the various interfaces that are multiplexed on to the I/O pins.

19.10.1 SCSI Ports

SCSI-8 Port p0

The pins listed below are used by SCSI-8 Port p0 in 8-bit mode. These pins are also used by the SCSI-W port in 16-bit (wide) mode (see table 19-20).

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	$\overline{s0msg}$	in/out (Note 6)	Message, driven by target during message phase.
T18	$\overline{s0cd}$	$\overline{s0cd}$	in/out (Note 6)	Control/Data, driven by target to determine whether control or data information is on the bus.
T19	$\overline{s0io}$	$\overline{s0io}$	in/out (Note 6)	Input/Output, driven by target and indicates bus direction.
R19	$\overline{s0ack}$	$\overline{s0ack}$	out	Acknowledgement signal in the information transfer handshake.
T20	$\overline{s0req}$	$\overline{s0req}$	in	Request signal in the information transfer handshake.
R20	$\overline{s0atn}$	$\overline{s0atn}$	out	Attention condition indicator from ETRAX 100LX to target.
K19	s0sel	s0sel	out	Select or reselect signal from SCSI interface to SCSI buffer.
J20	$\overline{s0sel}$	$\overline{s0sel}$	in (Note 7)	-SEL signal from SCSI bus to SCSI interface.
K20	s0bsy	s0bsy	out	Bus in use signal from SCSI interface to SCSI buffer.
K18	$\overline{s0bsy}$	$\overline{s0bsy}$	in (Note 7)	-BSY signal from SCSI bus to SCSI interface.
P17	s0rst	s0rst	out	Bus reset signal from SCSI interface to SCSI buffer.
R18	$\overline{s0rst}$	$\overline{s0rst}$	in (Note 7)	-RST signal from SCSI bus to SCSI interface.
N18	$\overline{s0p}$	$\overline{s0p}$	in/out	Data bus parity.
L20	$\overline{s0d0}$	$\overline{s0d0}$	in/out	Data bus of port p0 in SCSI 8-bit mode.
L18	$\overline{s0d1}$	$\overline{s0d1}$	in/out	
L19	$\overline{s0d2}$	$\overline{s0d2}$	in/out	
M19	$\overline{s0d3}$	$\overline{s0d3}$	in/out	
M18	$\overline{s0d4}$	$\overline{s0d4}$	in/out	
M17	$\overline{s0d5}$	$\overline{s0d5}$	in/out	
N20	$\overline{s0d6}$	$\overline{s0d6}$	in/out	
N19	$\overline{s0d7}$	$\overline{s0d7}$	in/out	
P20	s0oe	s0oe	out	External bus driver direction for signals $\overline{s0d0}$ to $\overline{s0d7}$ and $\overline{s0p}$.
P19	$\overline{s0en}$	$\overline{s0en}$	out	External driver output enable for signals $\overline{s0ack}$ and $\overline{s0atn}$.
W17	pb4	$\overline{s0enph}$	in/out	SCSI-0 phase enable for software ID select.

Table 19-20 SCSI-8 Port p0 Signals

For Notes 6 and 7, refer to *SCSI-W Port* on page 566.

SCSI-8 Port p1

The pins listed below are used by SCSI-8 Port p1 in 8-bit mode. Some pins are also used by the SCSI-W Port in 16-bit (wide) mode (see tables 19-20, 19-21, and 19-22).

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
D20	$\overline{\text{s1msg}}$	$\overline{\text{s1msg}}$	in/out (Note 6)	Message, driven by target during message phase.
E18	$\overline{\text{s1cd}}$	$\overline{\text{s1cd}}$	in/out (Note 6)	Control/Data, driven by target to determine whether control or data information is on the bus.
D19	$\overline{\text{s1io}}$	$\overline{\text{s1io}}$	in/out (Note 6)	Input/Output, driven by target and indicates bus direction.
B20	$\overline{\text{s1ack}}$	$\overline{\text{s1ack}}$	out	Acknowledgement signal in the information transfer handshake.
E17	$\overline{\text{s1req}}$	$\overline{\text{s1req}}$	in	Request signal in the information transfer handshake.
C18	$\overline{\text{s1atn}}$	$\overline{\text{s1atn}}$	out	Attention condition indicator from ETRAX 100LX to target.
H20	s1sel	s1sel	out	Select or reselect signal from SCSI interface to SCSI buffer.
J18	$\overline{\text{s1sel}}$	$\overline{\text{s1sel}}$	in (Note 7)	-SEL signal from SCSI bus to SCSI interface.
J17	s1bsy	s1bsy	out	Bus in use signal from SCSI interface to SCSI buffer.
J19	$\overline{\text{s1bsy}}$	$\overline{\text{s1bsy}}$	in (Note 7)	-BSY signal from SCSI bus to SCSI interface.
C19	s1rst	s1rst	out	Bus reset signal from SCSI interface to SCSI buffer.
C20	$\overline{\text{s1rst}}$	$\overline{\text{s1rst}}$	in (Note 7)	-RST signal from SCSI bus to SCSI interface.
E19	$\overline{\text{s1p}}$	$\overline{\text{s1p}}$	in/out	Data bus parity.
G17	$\overline{\text{s1d0}}$	$\overline{\text{s1d0}}$	in/out	Data bus of port p1 in SCSI 8-bit mode.
E20	$\overline{\text{s1d1}}$	$\overline{\text{s1d1}}$	in/out	
F19	$\overline{\text{s1d2}}$	$\overline{\text{s1d2}}$	in/out	
G18	$\overline{\text{s1d3}}$	$\overline{\text{s1d3}}$	in/out	
G19	$\overline{\text{s1d4}}$	$\overline{\text{s1d4}}$	in/out	
G20	$\overline{\text{s1d5}}$	$\overline{\text{s1d5}}$	in/out	
H18	$\overline{\text{s1d6}}$	$\overline{\text{s1d6}}$	in/out	
H19	$\overline{\text{s1d7}}$	$\overline{\text{s1d7}}$	in/out	
A20	s1oe	s1oe	out	External bus driver direction for signals $\overline{\text{s1d0}}$ to $\overline{\text{s1d7}}$ and $\overline{\text{s1p}}$.
B19	$\overline{\text{s1en}}$	$\overline{\text{s1en}}$	out	External driver output enable for signals $\overline{\text{s1ack}}$ and $\overline{\text{s1atn}}$.
U16	pb7	$\overline{\text{s1enph}}$	in/out	SCSI-1 phase enable for software ID select.

Table 19-21 SCSI-8 Port p1 Signals

For Notes 6 and 7, refer to *SCSI-W Port* on page 566.

SCSI-W Port

In 16-bit mode the SCSI-W Port uses the following I/O pins, which are also used by SCSI-8 Ports p0 and p1 in 8-bit mode.

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	$\overline{s0msg}$	in/out (Note 6)	Message, driven by target during message phase.
T18	$\overline{s0cd}$	$\overline{s0cd}$	in/out (Note 6)	Control/Data, driven by target to determine whether control or data information is on the bus.
T19	$\overline{s0io}$	$\overline{s0io}$	in/out (Note 6)	Input/output driven by target to show bus direction.
R19	$\overline{s0ack}$	$\overline{s0ack}$	out	Acknowledge signal in transfer handshake.
T20	$\overline{s0req}$	$\overline{s0req}$	in	Request signal in the information transfer handshake.
R20	$\overline{s0atn}$	$\overline{s0atn}$	out	Attention condition indicator from ETRAX 100LX to target.
K19	s0sel	s0sel	out	Select or reselect signal from SCSI interface to SCSI buffer.
J20	$\overline{s0sel}$	$\overline{s0sel}$	in (Note 7)	-SEL signal from SCSI bus to SCSI interface.
K20	s0bsy	s0bsy	out	Bus in use signal from SCSI interface to SCSI buffer.
J17	s1bsy	$\overline{s0enhiid}$	out	Enable arbitration ID 7 - 0 for software ID.
K18	$\overline{s0bsy}$	$\overline{s0bsy}$	in (Note 7)	-BSY signal from SCSI bus to SCSI interface.
P17	s0rst	s0rst	out	Bus reset signal from SCSI interface to SCSI buffer.
R18	$\overline{s0rst}$	$\overline{s0rst}$	in (Note 7)	-RST signal from SCSI bus to SCSI interface.
N18	$\overline{s0p}$	$\overline{s0p}$	in/out	Data bus low byte parity.
E19	$\overline{s1p}$	$\overline{s0p1}$	in/out	Data bus high byte parity.
L20	$\overline{s0d0}$	$\overline{s0d0}$	in/out	Low byte of data bus in SCSI-W mode.
L18	$\overline{s0d1}$	$\overline{s0d1}$	in/out	
L19	$\overline{s0d2}$	$\overline{s0d2}$	in/out	
M19	$\overline{s0d3}$	$\overline{s0d3}$	in/out	
M18	$\overline{s0d4}$	$\overline{s0d4}$	in/out	
M17	$\overline{s0d5}$	$\overline{s0d5}$	in/out	
N20	$\overline{s0d6}$	$\overline{s0d6}$	in/out	
N19	$\overline{s0d7}$	$\overline{s0d7}$	in/out	
G17	$\overline{s1d0}$	$\overline{s0d8}$	in/out	High byte of data bus in SCSI-W mode.
E20	$\overline{s1d1}$	$\overline{s0d9}$	in/out	
F19	$\overline{s1d2}$	$\overline{s0d10}$	in/out	
G18	$\overline{s1d3}$	$\overline{s0d11}$	in/out	
G19	$\overline{s1d4}$	$\overline{s0d12}$	in/out	
G20	$\overline{s1d5}$	$\overline{s0d13}$	in/out	
H18	$\overline{s1d6}$	$\overline{s0d14}$	in/out	
H19	$\overline{s1d7}$	$\overline{s0d15}$	in/out	
P20	s0oe	s0oe	out	External bus driver direction for $\overline{s0d0}$ to $\overline{s0d7}$ and $\overline{s0p}$.
A20	s1oe	s1oe	out	External bus driver direction for $\overline{s0d8}$ to $\overline{s0d15}$ and $\overline{s1p}$.
P19	$\overline{s0en}$	$\overline{s0en}$	out	External driver output enable for $\overline{s0ack}$ and $\overline{s0atn}$.
W17	pb4	$\overline{s0enph}$	in/out	SCSI-0 phase enable for software ID select.
U16	pb7	s0enloid	in/out	Enable arbitration ID 15 - 8 for software ID.

Table 19-22 SCSI-W Signals

Note 6: If software ID is enabled, the host SCSI ID number is driven to external logic during arbitration. Please refer to the information about the software ID and external buffer solution in Chapter 10.

Note 7: These OR-gated SCSI bus signals are generated by the external SCSI buffer.

19.10.2 ATA

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	iordy	in	I/O ready.
T18	$\overline{s0cd}$	dmarq0	in	DMA request bus 0.
T19	$\overline{s0io}$	dmarq1	in	DMA request bus 1.
T20	$\overline{s0req}$	dmarq2	in	DMA request bus 2.
R18	$\overline{s0rst}$	dmarq3	in	DMA request bus 3.
P17	s0rst	$\overline{cs0}$	out	Chip select 0.
R19	$\overline{s0ack}$	$\overline{cs1}$	out	Chip select 1.
R20	$\overline{s0atn}$	a0	out	Device address bit 0.
K20	s0bsy	a1	out	Device address bit 1.
P20	s0oe	a2	out	Device address bit 2.
N18	$\overline{s0p}$	$\overline{dmack0}$	out	DMA acknowledge bus 0.
E19	s1p	$\overline{dmack1}$	out	DMA acknowledge bus 1.
D20	$\overline{s1msg}$	$\overline{dmack2}$	out	DMA acknowledge bus 2.
E18	$\overline{s1cd}$	$\overline{dmack3}$	out	DMA acknowledge bus 3.
L20	$\overline{s0d0}$	d0	in/out	16-bit data bus of ATA port.
L18	$\overline{s0d1}$	d1	in/out	
L19	$\overline{s0d2}$	d2	in/out	
M19	$\overline{s0d3}$	d3	in/out	
M18	$\overline{s0d4}$	d4	in/out	
M17	$\overline{s0d5}$	d5	in/out	
N20	$\overline{s0d6}$	d6	in/out	
N19	$\overline{s0d7}$	d7	in/out	
G17	$\overline{s1d0}$	d8	in/out	
E20	$\overline{s1d1}$	d9	in/out	
F19	$\overline{s1d2}$	d10	in/out	
G18	$\overline{s1d3}$	d11	in/out	
G19	$\overline{s1d4}$	d12	in/out	
G20	$\overline{s1d5}$	d13	in/out	
H18	$\overline{s1d6}$	d14	in/out	
H19	$\overline{s1d7}$	d15	in/out	
P19	s0en	$\overline{dior0}$	out	Read strobe signal 0.
K19	s0sel	$\overline{dior1}$	out	Read strobe signal 1.
B19	s1en	$\overline{dior2}$	out	Read strobe signal 2.
H20	s1sel	$\overline{dior3}$	out	Read strobe signal 3.
K18	$\overline{s0bsy}$	intrq0	in	Interrupt request bus 0.
J20	$\overline{s0sel}$	intrq1	in	Interrupt request bus 1.
J19	$\overline{s1bsy}$	intrq2	in	Interrupt request bus 2.
J18	$\overline{s1sel}$	intrq3	in	Interrupt request bus 3.
C19	s1rst	$\overline{diow0}$	out	Write strobe signal 0.
B20	$\overline{s1ack}$	$\overline{diow1}$	out	Write strobe signal 1.
C18	s1atn	$\overline{diow2}$	out	Write strobe signal 2.
J17	s1bsy	$\overline{diow3}$	out	Write strobe signal 3.
A20	s1oe	ext_oe	out	Output enable for external driver.

Table 19-23 ATA Signals

19.10.3 Parallel Ports

Parallel Port p0

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description (Note 8)
V20	$\overline{s0msg}$	p0perror	in	Peripheral error signal to parallel port p0.
T18	$\overline{s0cd}$	$\overline{p0ack}$	in	Peripheral acknowledgement signal to parallel port p0.
T19	$\overline{s0io}$	p0busy	in	Peripheral busy signal to parallel port p0.
T20	$\overline{s0req}$	$\overline{p0fault}$	in	Peripheral fault signal to parallel port p0.
R18	$\overline{s0rst}$	p0select	in	Peripheral select signal to parallel port p0.
P17	s0rst	p0data_oe	out	Data output enable from parallel port p0.
R19	$\overline{s0ack}$	$\overline{p0selectin}$	out	Select in signal from parallel port p0.
R20	$\overline{s0atn}$	$\overline{p0autofd}$	out	Autofeed signal from parallel port p0.
K20	s0bsy	$\overline{p0strobe}$	out	Strobe signal from parallel port p0.
P20	s0oe	$\overline{p0init}$	out	Initialization signal from parallel port p0.
L20	$\overline{s0d0}$	p0d0	in/out	8-bit data bus of parallel port p0.
L18	$\overline{s0d1}$	p0d1	in/out	
L19	$\overline{s0d2}$	p0d2	in/out	
M19	$\overline{s0d3}$	p0d3	in/out	
M18	$\overline{s0d4}$	p0d4	in/out	
M17	$\overline{s0d5}$	p0d5	in/out	
N20	$\overline{s0d6}$	p0d6	in/out	
N19	$\overline{s0d7}$	p0d7	in/out	

Table 19-24 Parallel Port p0 Signals

Parallel Port p1

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description (Note 8)
D20	$\overline{s1msg}$	p1perror	in	Peripheral error signal to parallel port p1.
E18	$\overline{s1cd}$	$\overline{p1ack}$	in	Peripheral acknowledgement signal to parallel port p1.
D19	$\overline{s1io}$	p1busy	in	Peripheral busy signal to parallel port p1.
E17	$\overline{s1req}$	$\overline{p1fault}$	in	Peripheral fault signal to parallel port p1.
C20	$\overline{s1rst}$	p1select	in	Peripheral select signal to parallel port p1.
C19	s1rst	p1data_oe	out	Data output enable from parallel port p1.
B20	$\overline{s1ack}$	$\overline{p1selectin}$	out	Select in signal from parallel port p1.
C18	$\overline{s1atn}$	$\overline{p1autofd}$	out	Autofeed signal from parallel port p1.
J17	s1bsy	$\overline{p1strobe}$	out	Strobe signal from parallel port p1.
A20	s1oe	$\overline{p1init}$	out	Initialization signal from parallel port p1.
G17	$\overline{s1d0}$	p1d0	in/out	8-bit data bus of parallel port p1.
E20	$\overline{s1d1}$	p1d1	in/out	
F19	$\overline{s1d2}$	p1d2	in/out	
G18	$\overline{s1d3}$	p1d3	in/out	
G19	$\overline{s1d4}$	p1d4	in/out	
G20	$\overline{s1d5}$	p1d5	in/out	
H18	$\overline{s1d6}$	p1d6	in/out	
H19	$\overline{s1d7}$	p1d7	in/out	

Table 19-25 Parallel Port p1 Signals

Note 8: These descriptions apply to Centronics (Compatibility) mode only, which is the default mode of the parallel ports. For descriptions of these signals in other IEEE 1284 modes, please refer to *chapter 13 Parallel Ports*

Parallel Port-W (16-bit wide)

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	p0perror	in	Peripheral acknowledge signal to $\overline{p0init}$.
T18	$\overline{s0cd}$	$\overline{p0ack}$	in	Handshake signal in reverse mode.
T19	$\overline{s0io}$	p0busy	in	Flow control signal in the forward direction.
T20	$\overline{s0req}$	$\overline{p0fault}$	in	Interrupt request from peripheral.
R18	$\overline{s0rst}$	p0select	in	Indicates the ECP mode support.
P17	s0rst	p0data_oe	out	Data output enable signal.
R19	$\overline{s0ack}$	$\overline{p0selectin}$	out	Negotiation signal.
R20	$\overline{s0atn}$	$\overline{p0autofd}$	out	Flow control signal in the reverse direction.
K20	s0bsy	$\overline{p0strobe}$	out	Handshake signal in forward mode.
P20	s0oe	$\overline{p0init}$	out	Indicates the reverse mode when asserted (low).
L20	$\overline{s0d0}$	p0d0	in/out	16-bit data bus of parallel port-W.
L18	$\overline{s0d1}$	p0d1	in/out	
L19	$\overline{s0d2}$	p0d2	in/out	
M19	$\overline{s0d3}$	p0d3	in/out	
M18	$\overline{s0d4}$	p0d4	in/out	
M17	$\overline{s0d5}$	p0d5	in/out	
N20	$\overline{s0d6}$	p0d6	in/out	
N19	$\overline{s0d7}$	p0d7	in/out	
G17	$\overline{s1d0}$	p0d8	in/out	
E20	$\overline{s1d1}$	p0d9	in/out	
F19	$\overline{s1d2}$	p0d10	in/out	
G18	$\overline{s1d3}$	p0d11	in/out	
G19	$\overline{s1d4}$	p0d12	in/out	
G20	$\overline{s1d5}$	p0d13	in/out	
H18	$\overline{s1d6}$	p0d14	in/out	
H19	$\overline{s1d7}$	p0d15	in/out	

Table 19-26 Parallel Port-W Signals

19.10.4 Shared RAM and Shared RAM-W

Shared RAM

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	pr_adr0	in	Address bit 0, internally multiplexed with internally generated address bits.
T18	$\overline{s0cd}$	pr_adr1	in	Address bit 1, internally multiplexed with internally generated address bits.
T19	$\overline{s0io}$	\overline{intio}	in	Interrupt from peripheral.
T20	$\overline{s0req}$	rd_wr	in	Read/write select.
R18	$\overline{s0rst}$	$\overline{pr_req}$	in	Request from peripheral.
P17	s0rst	$\overline{pr_int}$	out	Interrupt to peripheral.
R19	$\overline{s0ack}$	$\overline{pr_ack}$	out	Acknowledgement to peripheral.
R20	$\overline{s0atn}$	a_sel	out	Address select for externally multiplexed address bits. High for address from external device.
L20	$\overline{s0d0}$	pr_d0	in/out	Data bus.
L18	$\overline{s0d1}$	pr_d1	in/out	
L19	$\overline{s0d2}$	pr_d2	in/out	
M19	$\overline{s0d3}$	pr_d3	in/out	
M18	$\overline{s0d4}$	pr_d4	in/out	
M17	$\overline{s0d5}$	pr_d5	in/out	
N20	$\overline{s0d6}$	pr_d6	in/out	
N19	$\overline{s0d7}$	pr_d7	in/out	

Table 19-27 Shared RAM Signals

Shared RAM-W

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V20	$\overline{s0msg}$	pr_adr0	in	Address bit 0, internally multiplexed with internally generated address bits.
T18	$\overline{s0cd}$	pr_adr1	in	Address bit 1, internally multiplexed with internally generated address bits.
T19	$\overline{s0io}$	\overline{intio}	in	Interrupt from peripheral.
T20	$\overline{s0req}$	rd_wr	in	Read/write select.
R18	$\overline{s0rst}$	$\overline{pr_req}$	in	Request from peripheral.
P17	$\overline{s0rst}$	$\overline{pr_int}$	out	Interrupt to peripheral.
R19	$\overline{s0ack}$	$\overline{pr_ack}$	out	Acknowledgement to peripheral.
R20	$\overline{s0atn}$	a_sel	out	Address select for externally multiplexed address bits. High for address from external device.
L20	$\overline{s0d0}$	pr_d0	in/out	Data bus low byte.
L18	$\overline{s0d1}$	pr_d1	in/out	
L19	$\overline{s0d2}$	pr_d2	in/out	
M19	$\overline{s0d3}$	pr_d3	in/out	
M18	$\overline{s0d4}$	pr_d4	in/out	
M17	$\overline{s0d5}$	pr_d5	in/out	
N20	$\overline{s0d6}$	pr_d6	in/out	
N19	$\overline{s0d7}$	pr_d7	in/out	
G17	$\overline{s1d0}$	pr_d8	in/out	Data bus high byte.
E20	$\overline{s1d1}$	pr_d9	in/out	
F19	$\overline{s1d2}$	pr_d10	in/out	
G18	$\overline{s1d3}$	pr_d11	in/out	
G19	$\overline{s1d4}$	pr_d12	in/out	
G20	$\overline{s1d5}$	pr_d13	in/out	
H18	$\overline{s1d6}$	pr_d14	in/out	
H19	$\overline{s1d7}$	pr_d15	in/out	

Table 19-28 Shared RAM-W Signals

19.10.5 Asynchronous Serial Ports

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
U19	txd1	txd1	out	Transmit data from Asynchronous Serial Port p1.
W20	$\overline{\text{rts1}}$	$\overline{\text{rts1}}$	out	Request to send from Asynchronous Serial Port p1.
T17	rxd1	rxd1	in	Receive data at Asynchronous Serial Port p1.
V19	$\overline{\text{cts1}}$	$\overline{\text{cts1}}$	in	Clear to send at Asynchronous Serial Port p1.
P19	$\overline{\text{s0en}}$	$\overline{\text{rts2}}$	out	Request to send from Asynchronous Serial Port p2.
K19	s0sel	txd2	out	Transmit data to Asynchronous Serial Port p2.
K18	$\overline{\text{s0bsy}}$	$\overline{\text{cts2}}$	in	Clear to send to Asynchronous Serial Port p2.
J20	$\overline{\text{s0sel}}$	rxd2	in	Receive data at Asynchronous Serial Port p2.
J19	$\overline{\text{s1bsy}}$	$\overline{\text{cts3}}$	in	Clear to send to Asynchronous Serial Port p3.
J18	$\overline{\text{s1sel}}$	rxd3	in	Receive data at Asynchronous Serial Port p3.
B19	$\overline{\text{s1en}}$	$\overline{\text{rts3}}$	out	Request to send from Asynchronous Serial Port p3.
H20	s1sel	txd3	out	Transmit data from Asynchronous Serial Port p3.

Table 19-29 Asynchronous Serial Ports p1, p2 and p3 Signals

19.10.6 Synchronous Serial Ports p1 and p3

The synchronous serial ports have six different modes of operation:

Master Output;
Master Input;

Slave Output;
Slave Input;

Master Bidirectional;
Slave Bidirectional.

The signal names at the I/O pins differ, depending upon the mode in use. The following tables show the different I/O pin assignments of the two synchronous serial ports in each mode of operation.

SYNCHRONOUS SERIAL PORTS - MASTER OUTPUT MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	-	J18	$\overline{s1sel}$	-	ss1_in1 ss3_in1	Not used by the synchronous serial ports in Master Output mode.
V19	$\overline{cts1}$	ss1status	J19	$\overline{s1bsy}$	ss3status	ss1_in2 ss3_in2	Serial busy input to respective port.
U19	txd1	ss1clk	H20	s1sel	ss3clk	ss1_out1 ss3_out1	Serial clock output from respective port.
W20	$\overline{rts1}$	ss1data	B19	$\overline{s1en}$	ss3data	ss1_out2 ss3_out2	Serial data output from respective port.
W17	pb4	ss1frame	U16	pb7	ss3frame	ss1_io3 ss3_io3	Serial frame indicator output from respective port.

Table 19-30 Pin Assignments of Synchronous Serial Ports p1 and p3 in Master Output Mode

SYNCHRONOUS SERIAL PORTS - MASTER INPUT MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	ss1data	J18	$\overline{s1sel}$	ss3data	ss1_in1 ss3_in1	Serial data input to respective port.
V19	$\overline{cts1}$	ss1status	J19	$\overline{s1bsy}$	ss3status	ss1_in2 ss3_in2	Serial empty input to respective port.
U19	txd1	ss1clk	H20	s1sel	ss3clk	ss1_out1 ss3_out1	Serial clock output from respective port.
W20	$\overline{rts1}$	ss1frame	B19	$\overline{s1en}$	ss3frame	ss1_out2 ss3_out2	Serial frame indicator from respective port.
W17	pb4	-	U16	pb7	-	-	Not used by the synchronous serial ports in Master Input mode.

Table 19-31 Pin Assignments of Synchronous Serial Ports p1 and p3 in Master Input Mode

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SYNCHRONOUS SERIAL PORTS - SLAVE OUTPUT MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	ss1clk	J18	$\overline{s1sel}$	ss3clk	ss1_in1 ss3_in1	Serial clock input to respective port.
V19	$\overline{cts1}$	ss1frame	J19	$\overline{s1bsy}$	ss3frame	ss1_in2 ss3_in2	Serial frame indicator to respective port.
U19	txd1	ss1data	H20	s1sel	ss3data	ss1_out1 ss3_out1	Serial data output from respective port.
W20	$\overline{rts1}$	ss1status	B19	$\overline{s1en}$	ss3status	ss1_out2 ss3_out2	Serial empty output from respective port.
W17	pb4	-	U16	pb7	-	-	Not used by the synchronous serial ports in Slave Output mode.

Table 19-32 Pin Assignments of Synchronous Serial Ports p1 and p3 in Slave Output Mode

SYNCHRONOUS SERIAL PORTS - SLAVE INPUT MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	ss1clk	J18	$\overline{s1sel}$	ss3clk	ss1_in1 ss3_in1	Serial clock input to respective port.
V19	$\overline{cts1}$	ss1frame	J19	$\overline{s1bsy}$	ss3frame	ss1_in2 ss3_in2	Serial frame indicator to respective port.
U19	txd1	-	H20	s1sel	-	ss1_out1 ss3_out1	Not used by the synchronous serial ports in Slave Input mode.
W20	$\overline{rts1}$	ss1status	B19	$\overline{s1en}$	ss3status	ss1_out2 ss3_out2	Serial busy output from respective port.
W17	pb4	ss1data	U16	pb7	ss3data	ss1_io3 ss3_io3	Serial data input to respective port.

Table 19-33 Pin Assignments of Synchronous Serial Ports p1 and p3 in Slave Input Mode

SYNCHRONOUS SERIAL PORTS - MASTER BIDIRECTIONAL MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	ss1status	J18	$\overline{s1sel}$	ss3status	ss1_in1 ss3_in1	Serial busy input to respective port.
V19	$\overline{cts1}$	ss1idata	J19	$\overline{s1bsy}$	ss3idata	ss1_in2 ss3_in2	Serial data input to respective port.
U19	txd1	ss1clk	H20	s1sel	ss3clk	ss1_out1 ss3_out1	Serial clock output from respective port.
W20	$\overline{rts1}$	ss1odata	B19	$\overline{s1en}$	ss3odata	ss1_out2 ss3_out2	Serial data output from respective port.
W17	pb4	ss1frame	U16	pb7	ss3frame	ss1_io3 ss3_io3	Serial frame indicator output from respective port.

Table 19-34 Pin Assignments of Synchronous Serial Ports p1 and p3 in Master Bidirectional Mode

SYNCHRONOUS SERIAL PORTS - SLAVE BIDIRECTIONAL MODE							
Synchronous Serial Port p1			Synchronous Serial Port p3			Interface Signal Name	Description
Solder Ball	Chip Pin Name	Mode Signal Name	Solder Ball	Chip Pin Name	Mode Signal Name		
T17	rxd1	ss1clk	J18	$\overline{s1sel}$	ss3clk	ss1_in1 ss3_in1	Serial clock input to respective port.
V19	$\overline{cts1}$	ss1frame	J19	$\overline{s1bsy}$	ss3frame	ss1_in2 ss3_in2	Serial frame indicator to respective port.
U19	txd1	ss1status	H20	s1sel	ss3status	ss1_out1 ss3_out1	Serial busy output from respective port.
W20	$\overline{rts1}$	ss1odata	B19	$\overline{s1en}$	ss3odata	ss1_out2 ss3_out2	Serial data output from respective port.
W17	pb4	ss1idata	U16	pb7	ss3idata	ss1_io3 ss3_io3	Serial data input to respective port.

Table 19-35 Pin Assignments of Synchronous Serial Ports p1 and p3 in Slave Bidirectional Mode

19.10.7 USB

USB Port p1

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
U19	txd1	$\overline{\text{usb1_oe}}$	out	Output enable from USB Port p1.
W20	$\overline{\text{rts1}}$	usb1_speed	out	Speed indicator signal from USB Port p1.
T17	rx1d	usb1_rcv	in	Serial data input to USB Port p1.
V19	$\overline{\text{cts1}}$	usb1_vp	in	Plus (D+) input to USB Port p1.
Y17	pb2	usb1_vpo	out	Plus (D+) output from USB Port p1.
V16	pb3	usb1_vmo	out	Minus (D-) output from USB Port p1.
Y18	pb5	usb1_vm	in	Minus (D-) input to USB Port p1.

Table 19-36 USB Port p1 Signals

USB Port p2

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
D20	$\overline{\text{s1msg}}$	$\overline{\text{usb2_oe}}$	out	Output enable from USB Port p2.
E18	$\overline{\text{s1cd}}$	usb2_speed	out	Speed indicator signal from USB Port p2.
D19	$\overline{\text{s1io}}$	usb2_rcv	in	Serial data input to USB Port p2.
E17	$\overline{\text{s1req}}$	usb2_vp	in	Plus (D+) input to USB Port p2.
C18	$\overline{\text{s1atn}}$	usb2_vpo	out	Plus (D+) output from USB Port p2.
C20	$\overline{\text{s1rst}}$	usb2_vm	in	Minus (D-) input to USB Port p2.
J17	s1bsy	usb2_vmo	out	Minus (D-) output from USB Port p2.

Table 19-37 USB Port p2 Signals

19.10.8 Chip Selects for Peripherals (CSP)

The CSP port offers additional chip select signals for use with peripheral devices.

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
Y17	pb2	$\overline{\text{csp1}}$	out	Additional peripheral chip select signal 1.
V16	pb3	$\overline{\text{csp2}}$	out	Additional peripheral chip select signal 2.
W17	pb4	$\overline{\text{csp3}}$	out	Additional peripheral chip select signal 3.
Y18	pb5	$\overline{\text{csp5}}$	out	Additional peripheral chip select signal 5.
Y19	pb6	$\overline{\text{csp6}}$	out	Additional peripheral chip select signal 6.
U16	pb7	$\overline{\text{csp7}}$	out	Additional peripheral chip select signal 7.

Table 19-38 CSP Signals

19.10.9 I2C

Solder Ball	Chip Pin Name	Interface Pin Name	Direction	Description
V15	pb0	i2c_d	in/out	I2C data input/output.
W16	pb1	i2c_clk	out	I2C output clock signal.

Table 19-39 I2C Signals

19.10.10 General Port PB

Solder Ball	Name	Direction	Description
V15	pb0	in/out	General Port PB, bit 0.
W16	pb1	in/out	General Port PB, bit 1.
Y17	pb2	in/out	General Port PB, bit 2.
V16	pb3	in/out	General Port PB, bit 3.
W17	pb4	in/out	General Port PB, bit 4.
Y18	pb5	in/out	General Port PB, bit 5.
Y19	pb6	in/out	General Port PB, bit 6.
U16	pb7	in/out	General Port PB, bit 7.

Table 19-40 General Port PB Signals

19.11 I/O Pin Default Values

All bidirectional ports are input by default. The output pins have the default values given in the table below.

Solder Ball	Default Value	Chip Pin Name	Interface Pin Name						
			SCSI	Serial Ports	ATA	Parallel Ports	Shared RAM	Gen I/O	USB
P17	0	s0rst	s0rst		cs0	p0data_oe	pr_int	g5	
R19	0	s0ack	s0ack		cs1	p0selectin	pr_ack	g4	
R20	0	s0atn	s0atn		a0	p0autofd	a_sel	g3	
K20	0	s0bsy	s0bsy		a1	p0strobe		g2	
P20	0	s0oe	s0oe		a2	p0init		g1	
P19	1	s0en	s0en	rts2	dior0			g7	
K19	No default (Note 9)	s0sel	s0sel	txd2	dior1			g6	
B19	1	s1en	s1en	rts3	dior2			g31	
H20	No default (Note 9)	s1sel	s1sel	txd3	dior3			g30	
C19	0	s1rst	s1rst		dior0	p1data_oe		g29	
B20	0	s1ack	s1ack		dior1	p1selectin		g28	
C18	0	s1atn	s1atn		dior2	p1autofd		g27	
J17	0	s1bsy	s1bsy		dior3	p1strobe		g26	
A20	0	s1oe	s1oe		ext_oe	p1init		g25	
Y7	1	txd0		txd0					
V8	1	rts0		rts0					
U19	1	txd1		txd1					usb_oe
W20	1	rts1		rts1					usb1_speed

Table 19-41 I/O Pin Default Values

Note 9: These pins have no default. Their condition depends upon the state of serial port hardware configuration signal hcfg as follows:

if (hcfg = 1), then {s0sel = 0, s1sel = 0}
 if (hcfg = 0), then {s0sel = 1, s1sel = 1}

Signal hcfg is listed in Table 19-7.

19.12 DC Electrical Specifications

19.12.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage.	0	3.6	V
V_{in}	DC input voltage.	0	6.5	V
V_{out}	DC off-state output voltage.	0	6.5	V
T_{stg}	Storage temperature.	-65	150	°C
T_A	Operating temperature.	0	70	°C

Table 19-42 Absolute Maximum Ratings

ESD protection: up to 2kV (Human Body Model according to the MIL-STD-883 method 3015).

Lead temperature: accords with the specification for a JEDEC Level 3 package.

19.12.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD}	DC supply voltage.	3.0	3.3	3.6	V
V_{in}	DC input voltage.	0	-	5.5	V
V_{out}	DC off-state output voltage.	0	-	5.5	V
T_A	Operating temp. (Ambient temp. range).	0	-	70	°C
I_{OH}	High level output current: pa0, pa1, pa2, pa3, pa4, pa5, pa6, pa7.	-	-	-12	mA
	All other.	-	-	-4	mA
I_{OL}	Low level output current: pa0, pa1, pa2, pa3, pa4, pa5, pa6, pa7.	-	-	12	mA
	All other.	-	-	4	mA

Table 19-43 Recommended Operating Conditions

19 Electrical Information

19.12.3 Capacitance

All pins have a typical capacitance of 5 pF and a maximum capacitance of 6 pF.

19.12.4 DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	High level input voltage, all inputs except clkin.	2.0	-	5.5	V
V_{IL}	Low level input voltage, all inputs except clkin.	0	-	0.8	V
V_{IH}	High level input voltage, clkin.	$0.7 \times V_{DD}$	-	5.5	V
V_{IL}	Low level input voltage, clkin.	0	-	$0.3 \times V_{DD}$	V
	Schmitt-trigger hysteresis. (See Table 19-45).	0.5	0.575	0.65	V
V_{OH}	High level output voltage.	2.4	-	V_{DD}	V
V_{OL}	Low level output voltage.	0	-	0.4	V
I_{in}	Input leakage current.	-10	-	10	μA
I_{ioz}	I/O leakage current.	-10	-	10	μA
I_{DD}	Supply current.	-	105	170	mA

Table 19-44 DC Electrical Characteristics

19.12.5 Input Buffer Types

Signal	Buffer Type
clkin.	CMOS
$\overline{cts0}$, \overline{irq} , \overline{nmi} , \overline{reset} , $\overline{rxd0}$.	TTL Schmitt Trigger
All other.	TTL

Table 19-45 Input Buffer Types

19.13 AC Electrical Specifications

This section provides the AC characteristics for the ETRAX 100LX. The timing sequences are related to the internal 100 MHz clock.

The table below lists all bus states used in the timing diagrams on the following pages.

Bus State Descriptions

State	Description	Comment
T_a	Activate state. The \overline{rd} , \overline{wr} or \overline{inta} strobes are asserted in this state. Signal \overline{cas} is asserted after the end of this state.	
T_d	Data state. "Data in" is sampled at the end of this state, except for EDO DRAM, where data is sampled 15 ns after the end of this state.	
T_z	Data bus turn-off state. This state is inserted between bursts, to allow the ETRAX 100LX and external units to turn off their outputs before the data bus is driven by another source. This state may overlap with a T_{ew} state.	
T_{pa}	Row address signal \overline{ras} precharge activate state. Signal \overline{ras} is set high after the end of this state.	
T_{pd}	Row address signal \overline{ras} precharge state. DRAM row address is asserted after the end of this state. During DRAM refresh, column address signal \overline{cas} is set low after the end of this state.	
T_{ra}	Row address signal \overline{ras} activate state. Signal \overline{ras} is set low after the end of this state.	
T_{rd}	Row address hold state.	
T_{be0}, T_{be1}	Burst end states. This is inserted at the end of an EDO DRAM read burst, to allow the last data of the burst to be sampled. These states may overlap with a T_{ew} state.	
T_{ew}	Early wait state. This state may overlap with a T_z , T_{zw} , T_{be0} , or T_{be1} state.	Inserted before T_a
T_{lw}	Late wait state.	Inserted between T_a and T_d
T_{zw}	Turn-off wait state. This state may overlap with a T_{ew} state.	Inserted after T_d
T_{xw}	External wait state.	
T_{xx}	Any bus state.	

Table 19-46 Bus State Descriptions

Wait States

The table below lists the wait state parameters used in the timing diagrams that follow. These parameters correspond to the wait state values described in Chapter 5.

Name	Description
ew	Number of early wait states.
lw	Number of late wait states.
zw	Number of turn-off wait states.
c	Column address signal $\overline{\text{cas}}$ delay.
cw	Number of $\overline{\text{cas}}$ wait states.
cp	Number of $\overline{\text{cas}}$ precharge wait states.
rp	Number of $\overline{\text{ras}}$ precharge wait states.
rs	Number of row address setup wait states.
rh	Number of row address hold wait states.
cz	Number of turn-off wait states after $\overline{\text{cas}}$.

Table 19-47 Wait States

19.13.1 Conditions

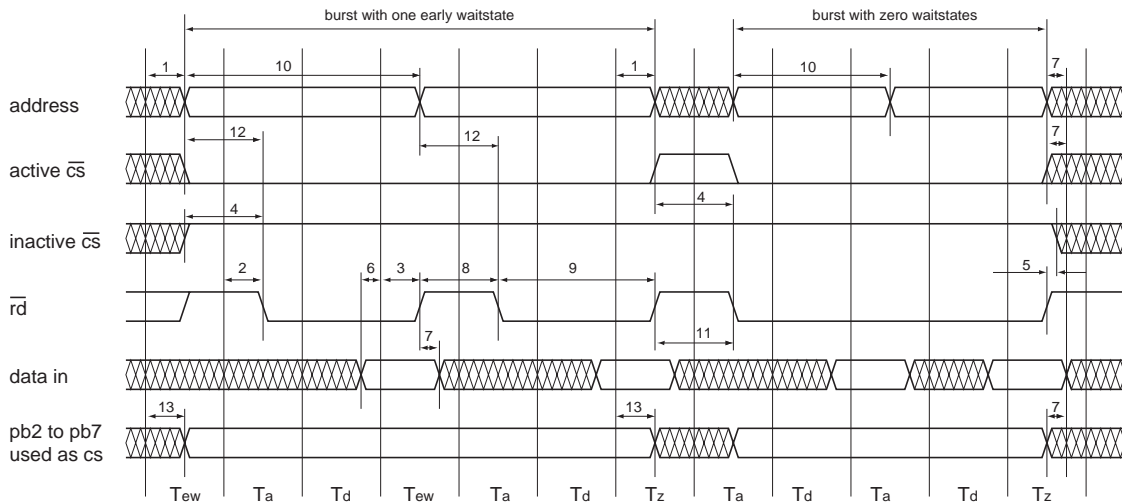
The timing information in the chapter is valid under the operating conditions given in the table below.

Condition	Value
T_A	0°C to 70°C
V_{DD}	3.3 V +/- 0.3 V
Capacitive load	50 pF

Table 19-48 Operating Conditions for Timing Information

19.13.2 SRAM/Flash/Peripheral Timing

Read Cycle



Active and inactive \overline{cs} are valid for $\overline{cse0}$, $\overline{cse1}$, $\overline{csr0}$, $\overline{csr1}$, $\overline{csp0}$ and $\overline{csp4}$.

Figure 19-2 SRAM/Flash/Peripheral - Read Cycle Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock. (Note 10).	2	-	8	-	ns
2	t_{rl}	Read low delay from clock.	2	-	8	-	ns
3	t_{rh}	Read high delay from clock.	2	-	7	-	ns
4	t_{cshr}	Chip select high to read low.	8	-	-	-	ns
5	t_{rhcs}	Read high to chip select low.	0	-	-	-	ns
6	t_{ds}	Data in setup time to clock.	0	-	-	-	ns
7	t_{dh}	Data hold time from address, chip select or read, whichever occurs first.	0	-	-	-	ns
8	t_{rhw}	Read inactive width within burst.	-2	-	-	10-ew	ns
9	t_{rw}	Read active width.	16	20	-	10-lw	ns
10	t_{rc}	Read cycle.	-	20	-	10-(ew+lw)	ns
11	t_{rhr}	Read inactive width after burst.	8	-	-	10-zw	ns
12	t_{ar}	Read inactive time after chip select or address.	-2	-	-	10-ew	ns
13	t_{pcs}	pb delay from clock when used as chip selects.	3	-	12	-	ns

Table 19-49 SRAM/Flash/Peripheral Read Cycle Timing

Note 10: Valid for $\overline{cse0}$, $\overline{cse1}$, $\overline{csr0}$, $\overline{csr1}$, $\overline{csp0}$ and $\overline{csp4}$.

Write Cycle, Normal Write

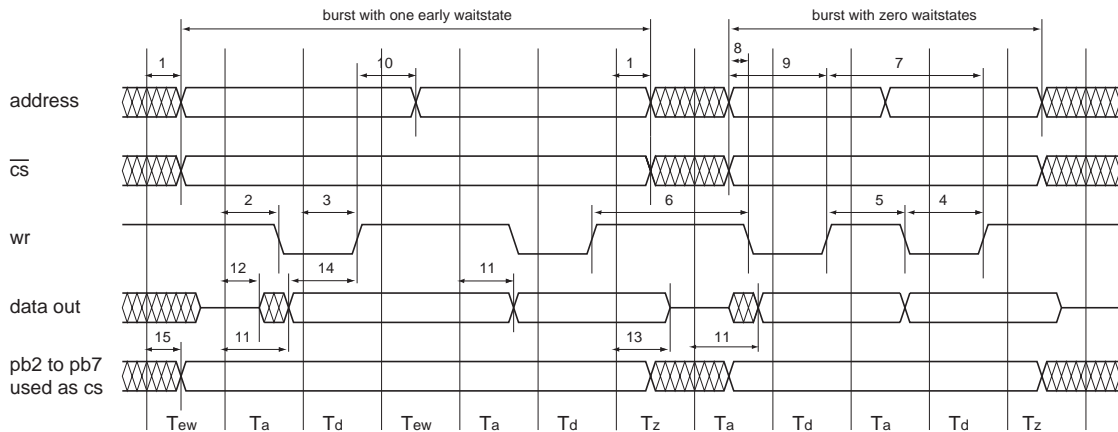


Figure 19-3 SRAM/Flash/Peripheral Write Cycle Timing Diagram - Normal Write

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock.	2	-	8	-	ns
2	t_{wl}	Write low delay from clock.	7	-	13	-	ns
3	t_{wh}	Write high delay from clock.	7	-	13	-	ns
4	t_{ww}	Write pulse width.	6	-	-	10·lw	ns
5	t_{whw}	Write inactive width within burst.	9	-	-	10·ew	ns
6	t_{whl}	Write inactive width after burst.	19	-	-	10·zw	ns
7	t_{wc}	Write cycle time.	-	20	-	10·(ew+lw)	ns
8	t_{awl}	Address and chip select setup to write low.	2	-	-	10·ew	ns
9	t_{awh}	Address and chip select setup to end of write.	11	-	-	10·(ew+lw)	ns
10	t_{ahw}	Address hold after write high.	3	-	-	-	ns
11	t_{do}	Data delay from clock.	6	-	13	-	ns
12	t_{doe}	Data turn on time from clock.	6	-	-	-	ns
13	t_{doz}	Data turn off time from clock.	6	-	10	10·zw	ns
14	t_{dwh}	Data valid to end of write.	6	-	-	10·lw	ns
15	t_{pcs}	pb delay from clock, when used as chip selects.	3	-	12	-	ns

Table 19-50 SRAM/Flash/Peripheral Write Cycle Timing - Normal Write

Write Cycle, Extended Write

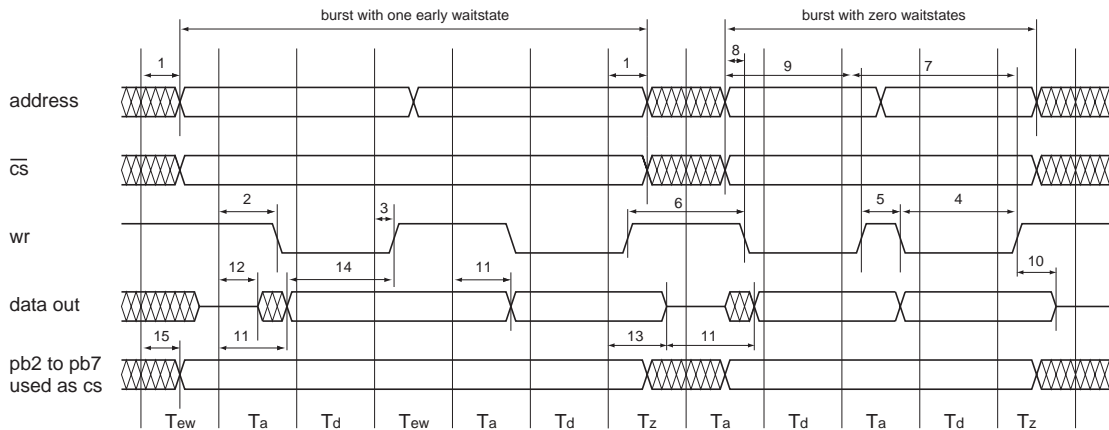


Figure 19-4 SRAM/Flash/Peripheral Write Cycle Timing Diagram - Extended Write

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock.	2	-	8	-	ns
2	t_{wl}	Write low delay from clock.	7	-	13	-	ns
3	t_{whx}	Write high delay from clock.	2	-	7	-	ns
4	t_{wwx}	Write pulse width.	11	-	-	10-lw	ns
5	t_{whwx}	Write inactive width within burst.	4	-	-	10-ew	ns
6	t_{whlx}	Write inactive width after burst.	13	-	-	10-zw	ns
7	t_{wcx}	Write cycle time.	-	20	-	10-(ew+lw)	ns
8	t_{awl}	Address and chip select setup to write low.	2	-	-	10-ew	ns
9	t_{awhx}	Address and chip select setup to end of write.	16	-	-	10-(ew+lw)	ns
10	t_{whdx}	Data hold after end of write.	2	-	-	10-ew within burst, 10-zw after burst	ns
11	t_{do}	Data delay from clock.	6	-	13	-	ns
12	t_{doe}	Data turn on time from clock.	6	-	-	-	ns
13	t_{doz}	Data turn off time from clock.	6	-	10	10-zw	ns
14	t_{dwhx}	Data valid to end of write.	11	-	-	10-lw	ns
15	t_{pcs}	pb delay from clock, when used as chip selects.	3	-	12	-	ns

Table 19-51 SRAM/Flash/Peripheral Write Cycle Timing - Extended Write Timing

19.13.3 Synchronous DRAM

50/100 MHz Mode, Read

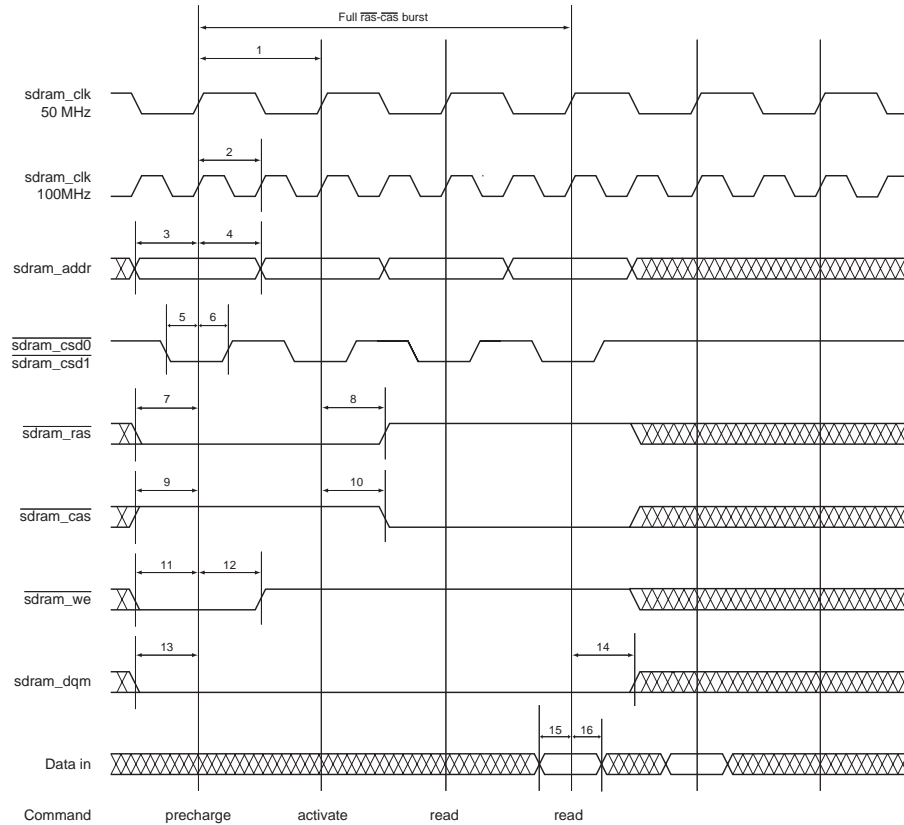


Figure 19-5 Synchronous DRAM, 50/100 MHz Mode - Read Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{sclks}	Clock period, 50 MHz mode	-	20	-	ns
2	t_{sclkf}	Clock period, 100 MHz mode	-	10	-	ns
3	t_{sas}	Address setup time to clock	9	-	-	ns
4	t_{sah}	Address hold time from clock	9	-	-	ns
5	t_{scs}	$\overline{sdr_csd0/1}$ setup time to clock	4	-	-	ns
6	t_{ch}	$\overline{sdr_csd0/1}$ hold time from clock.	4	-	-	ns
7	t_{rs}	$\overline{sdr_ras}$ setup time to clock	9	-	-	ns
8	t_{rh}	$\overline{sdr_ras}$ hold time from clock	9	-	-	ns
9	t_{scs}	$\overline{sdr_cas}$ setup time to clock	9	-	-	ns
10	t_{sch}	$\overline{sdr_cas}$ hold time from clock	9	-	-	ns
11	t_{sws}	$\overline{sdr_we}$ setup time to clock	9	-	-	ns
12	t_{swh}	$\overline{sdr_we}$ hold time from clock	9	-	-	ns
13	t_{sds}	$\overline{sdr_dqm}$ setup time to clock	9	-	-	ns
14	t_{sdh}	$\overline{sdr_dqm}$ hold time from clock	9	-	-	ns
15	t_{sdis}	Data in setup time to clock	1	-	-	ns
16	t_{sdih}	Data in hold time from clock	3	-	-	ns

Table 19-52 Synchronous DRAM, 50/100 MHz Mode - Read Timing

50/100 MHz Mode, Write

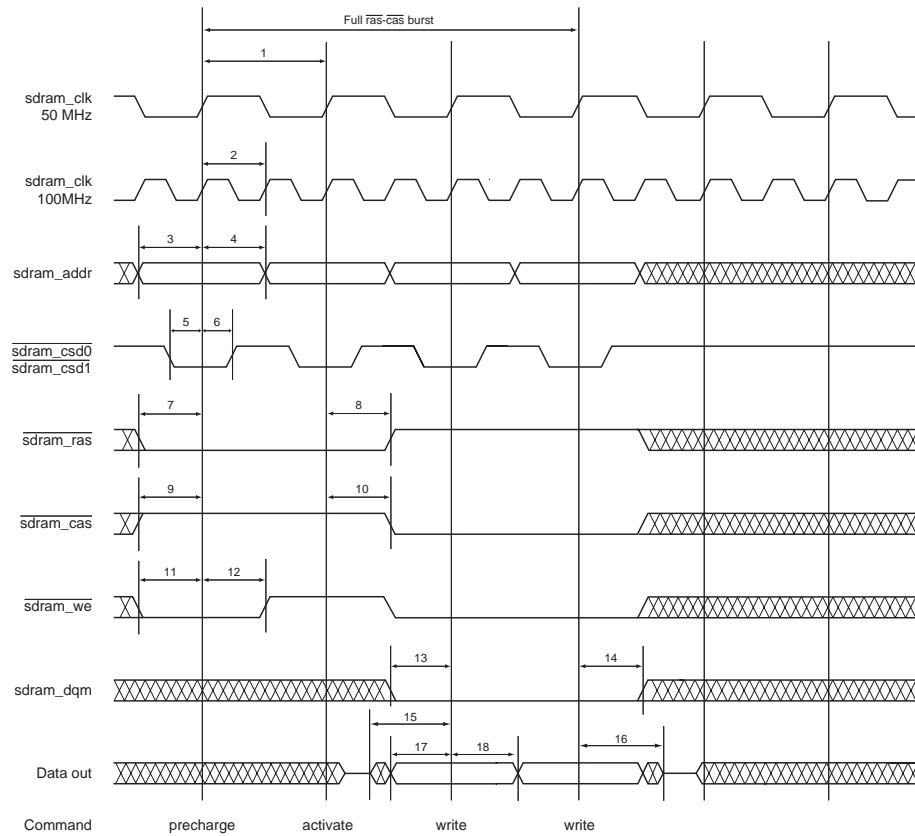


Figure 19-6 Synchronous DRAM, 50/100 MHz Mode - Write Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{sclks}	Clock period, 50 MHz mode	-	20	-	ns
2	t_{sclkf}	Clock period, 100 MHz mode	-	10	-	ns
3	t_{sas}	Address setup time to clock	9	-	-	ns
4	t_{sah}	Address hold time from clock	9	-	-	ns
5	t_{scs}	$\overline{\text{sdram_csd0/1}}$ setup time to clock	4	-	-	ns
6	t_{sch}	$\overline{\text{sdram_csd0/1}}$ hold time from clock.	4	-	-	ns
7	t_{srs}	$\overline{\text{sdram_ras}}$ setup time to clock	9	-	-	ns
8	t_{srh}	$\overline{\text{sdram_ras}}$ hold time from clock	9	-	-	ns
9	t_{scs}	$\overline{\text{sdram_cas}}$ setup time to clock	9	-	-	ns
10	t_{sch}	$\overline{\text{sdram_cas}}$ hold time from clock	9	-	-	ns
11	t_{sws}	$\overline{\text{sdram_we}}$ setup time to clock	9	-	-	ns
12	t_{swh}	$\overline{\text{sdram_we}}$ hold time from clock	9	-	-	ns
13	t_{sds}	sdram_dqm setup time to clock	9	-	-	ns
14	t_{sdh}	sdram_dqm hold time from clock	9	-	-	ns
15	t_{sdoe}	Data out turn on time to clock	-	-	11	ns
16	t_{sdoz}	Data out turn off time from clock	-	-	13	ns
17	t_{sdos}	Data out setup time to clock	7	-	-	ns
18	t_{sdoh}	Data out hold time from clock	9	-	-	ns

Table 19-53 Synchronous DRAM, 50/100 MHz Mode - Write Timing

DDR 100 MHz Mode, Read

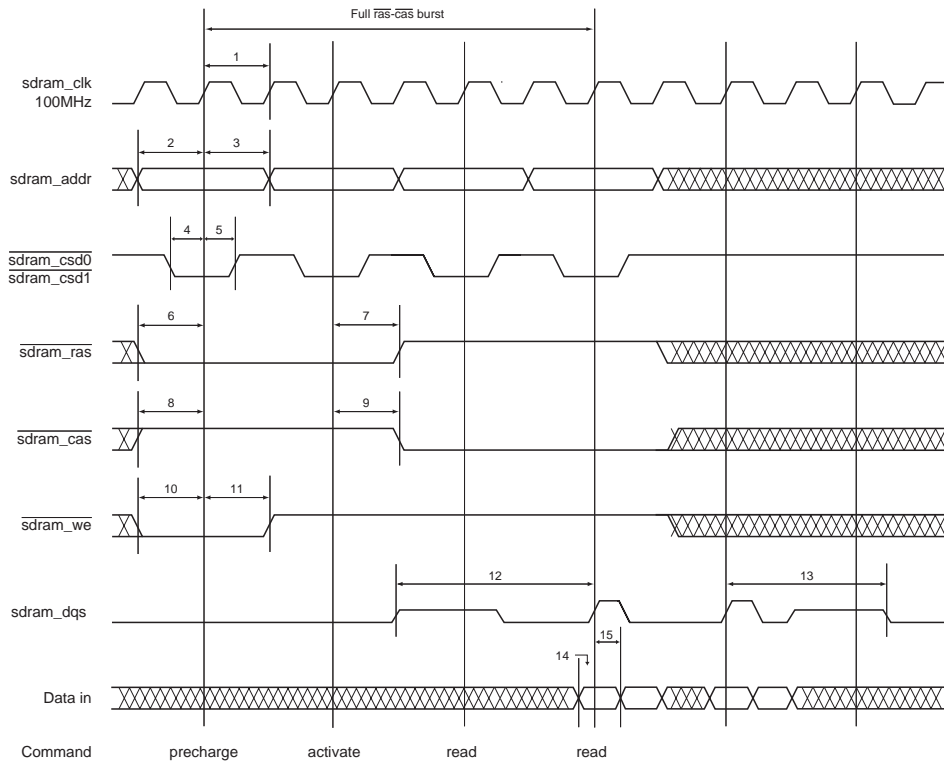


Figure 19-7 DDR 100 MHz Mode - Read Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{scklf}	Clock period	-	10	-	ns
2	t_{sas}	Address setup time to clock	9	-	-	ns
3	t_{sah}	Address hold time from clock	9	-	-	ns
4	t_{scs}	$\overline{sdr_csd0/1}$ setup time to clock	4	-	-	ns
5	t_{sch}	$\overline{sdr_csd0/1}$ hold time from clock.	4	-	-	ns
6	t_{srs}	$\overline{sdr_ras}$ setup time to clock	9	-	-	ns
7	t_{srh}	$\overline{sdr_ras}$ hold time from clock	9	-	-	ns
8	t_{scs}	$\overline{sdr_cas}$ setup time to clock	9	-	-	ns
9	t_{sch}	$\overline{sdr_cas}$ hold time from clock	9	-	-	ns
10	t_{sws}	$\overline{sdr_we}$ setup time to clock	9	-	-	ns
11	t_{swh}	$\overline{sdr_we}$ hold time from clock	9	-	-	ns
12	t_{dsdq}	sdr_dqs turn off time to clock	22	-	-	ns
13	t_{dsdqe}	sdr_dqs turn on time from clock	24	-	-	ns
14	t_{dsdis}	Data in setup time from sdr_dqs	-0.5	-	-	ns
15	t_{dsdih}	Data in hold time from sdr_dqs	3	-	-	ns

Table 19-54 DDR 100 MHz Mode - Read Timing

DDR 100 MHz Mode, Write

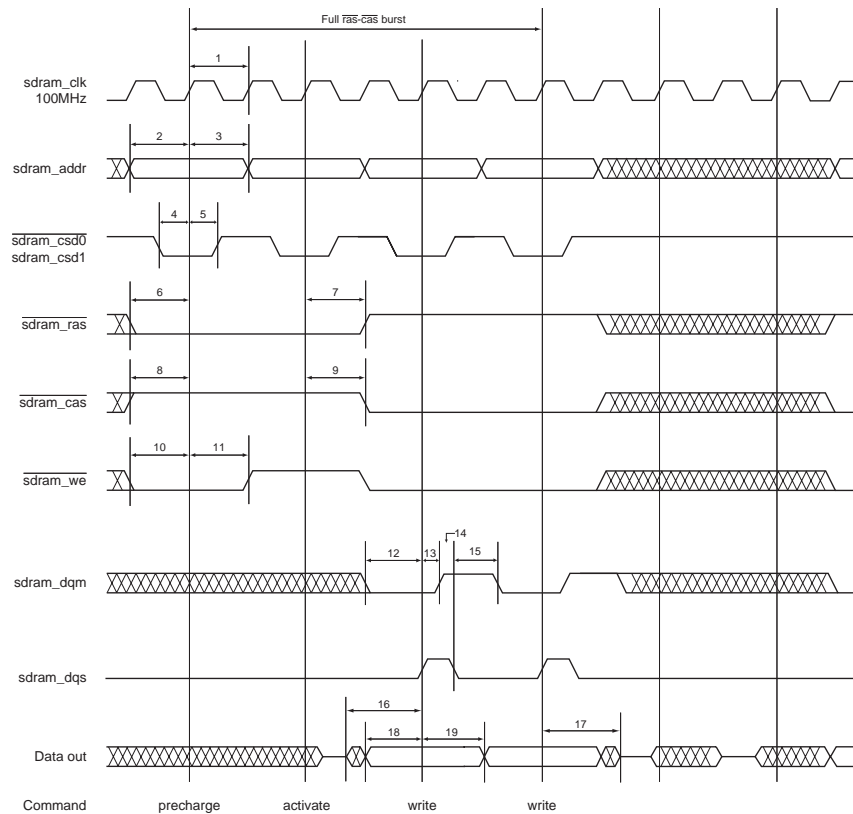


Figure 19-8 DDR 100 MHz Mode - Write Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{scklf}	Clock period	-	10	-	ns
2	t_{sas}	Address setup time to clock	9	-	-	ns
3	t_{sah}	Address hold time from clock	9	-	-	ns
4	t_{scs}	$\overline{\text{sdram_csd0/1}}$ setup time to clock	4	-	-	ns
5	t_{sch}	$\overline{\text{sdram_csd0/1}}$ hold time from clock.	4	-	-	ns
6	t_{srs}	$\overline{\text{sdram_ras}}$ setup time to clock	9	-	-	ns
7	t_{srh}	$\overline{\text{sdram_ras}}$ hold time from clock	9	-	-	ns
8	t_{scs}	$\overline{\text{sdram_cas}}$ setup time to clock	9	-	-	ns
9	t_{sch}	$\overline{\text{sdram_cas}}$ hold time from clock	9	-	-	ns
10	t_{sws}	$\overline{\text{sdram_we}}$ setup time to clock	9	-	-	ns
11	t_{swh}	$\overline{\text{sdram_we}}$ hold time from clock	9	-	-	ns
12	t_{dsdmsr}	sdram_dqm setup time to sdram_dqs rising edge	6	-	-	ns
13	t_{dsdmhr}	sdram_dqm hold time from sdram_dqs rising edge	2.5	-	-	ns
14	t_{dsdmsf}	sdram_dqm setup time to sdram_dqs falling edge	1.5	-	-	ns
15	t_{dsdmhf}	sdram_dqm hold time to sdram_dqs falling edge	8	-	-	ns
16	t_{dsdoe}	Data out turn on time to sdram_dqs	-	-	28	ns
17	t_{dsdoz}	Data out turn off time from sdram_dqs	-	-	3	ns
18	t_{dsdos}	Data out setup time to sdram_dqs	8	-	-	ns
19	t_{dsdoh}	Data out hold time from sdram_dqs	3	-	-	ns

Table 19-55 DDR 100 MHz Mode - Write Timing

19.13.4 Asynchronous DRAM

Fast Page Mode, Read

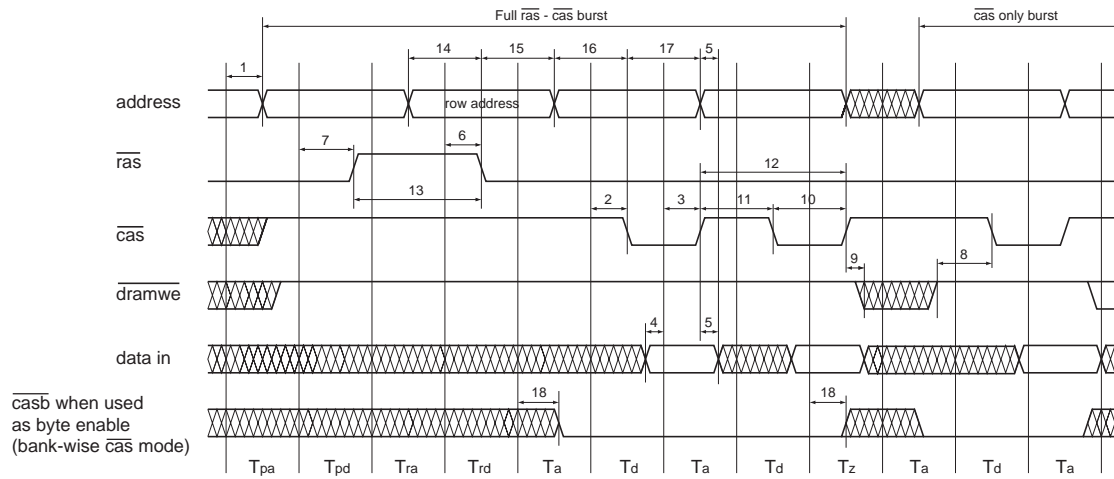


Figure 19-9 Asynchronous DRAM, Fast Page Mode - Read Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock.	2	-	8	-	ns
2	t_{casl}	\overline{cas} low delay from clock.	2	-	8	5-c	ns
3	t_{cash}	\overline{cas} high delay from clock.	2	-	8	-	ns
4	t_{ds}	Data in setup time to clock.	0	-	-	-	ns
5	t_{dh}	Data in hold time from \overline{cas} or address change, whichever occurs first.	0	-	-	-	ns
6	t_{rasl}	\overline{ras} low time from clock.	3	-	10	-	ns
7	t_{rash}	\overline{ras} high time from clock.	7	-	13	-	ns
8	t_{rcs}	\overline{dramwe} high setup time to \overline{cas} low.	4	-	-	5-c	ns
9	t_{rch}	\overline{dramwe} high hold time from \overline{cas} high.	2	-	-	-	ns
10	t_{cas}	\overline{cas} pulse width.	7	-	-	10-cw - 5-c	ns
11	t_{cp}	\overline{cas} precharge time.	7	-	-	10-cp + 5-c	ns
12	t_{pc}	\overline{cas} cycle time.	-	20	-	10·(cp + cw)	ns
13	t_{rp}	\overline{ras} precharge time.	14	-	-	10·(rp + rs)	ns
14	t_{asr}	Row address setup time to \overline{ras} .	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from \overline{ras} .	4	-	-	10-rh	ns
16	t_{asc}	Column address setup time to \overline{cas} .	7	-	-	10-cp + 5-c	ns
17	t_{cah}	Column address hold time from \overline{cas} .	7	-	-	10-cw - 5-c	ns
18	t_{be}	\overline{casb} delay from clock, when used as byte enable (bankwise mode).	2	-	8	-	ns

Table 19-56 Asynchronous DRAM, Fast Page Mode - Read Timing

EDO DRAM, Read

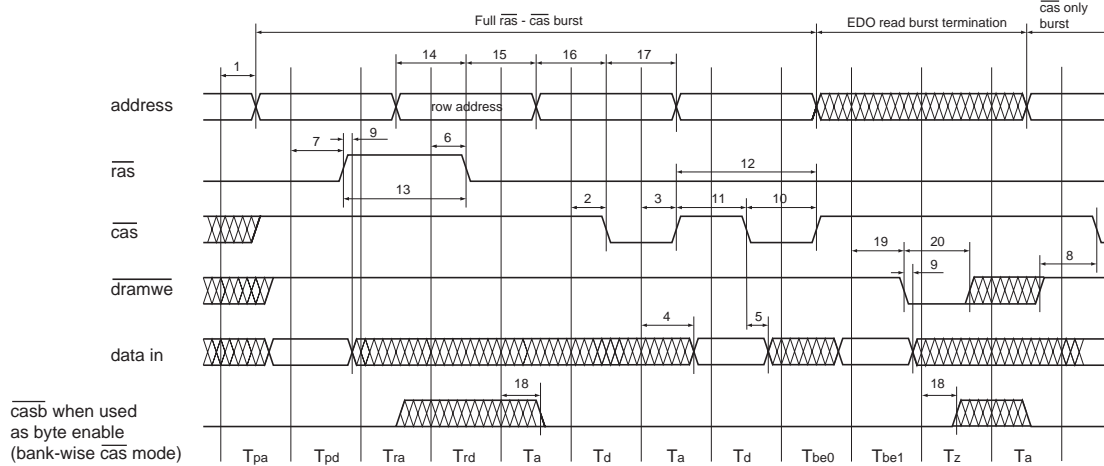


Figure 19-10 EDO DRAM - Read Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock.	2	-	8	-	ns
2	t_{casl}	$\overline{\text{cas}}$ low delay from clock.	2	-	8	5-c	ns
3	t_{cash}	$\overline{\text{cas}}$ high delay from clock.	2	-	8	-	ns
4	t_{dd}	Data in valid delay from clock.	-	-	15	-	ns
5	t_{coh}	Data in hold time from $\overline{\text{cas}}$ low.	4	-	-	(-10)·cp - 5-c	ns
6	t_{rasl}	$\overline{\text{ras}}$ low time from clock.	3	-	10	-	ns
7	t_{rash}	$\overline{\text{ras}}$ high time from clock.	8	-	13	-	ns
8	t_{rcs}	$\overline{\text{dramwe}}$ high setup time to $\overline{\text{cas}}$ low.	4	-	-	5-c	ns
9	t_{dh}	Data in hold time from $\overline{\text{dramwe}}$ low or $\overline{\text{ras}}$ high, whichever occurs first.	0	-	-	-	ns
10	t_{cas}	$\overline{\text{cas}}$ pulse width.	7	-	-	10-cw - 5-c	ns
11	t_{cp}	$\overline{\text{cas}}$ precharge time.	7	-	-	10-cp + 5-c	ns
12	t_{pc}	$\overline{\text{cas}}$ cycle time.	-	20	-	10·(cp + cw)	ns
13	t_{rp}	$\overline{\text{ras}}$ precharge time.	14	-	-	10·(rp + rs)	ns
14	t_{asr}	Row address setup time to $\overline{\text{cas}}$.	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from $\overline{\text{cas}}$.	4	-	12	10-rh	ns
16	t_{asc}	Column address setup time to $\overline{\text{cas}}$.	7	-	-	10-cp + 5-c	ns
17	t_{cah}	Column address hold time from $\overline{\text{cas}}$.	7	-	-	10-cw - 5-c	ns
18	t_{be}	$\overline{\text{casb}}$ delay from clock, when used as byte enable (bankwise mode).	2	-	8	-	ns
19	t_{wel}	$\overline{\text{dramwe}}$ low delay from clock.	7	-	13	-	ns
20	t_{wew}	$\overline{\text{dramwe}}$ pulse width after EDO read burst.	7	-	-	10-cz	ns

Table 19-57 EDO DRAM - Read Timing

Asynchronous DRAM, Write

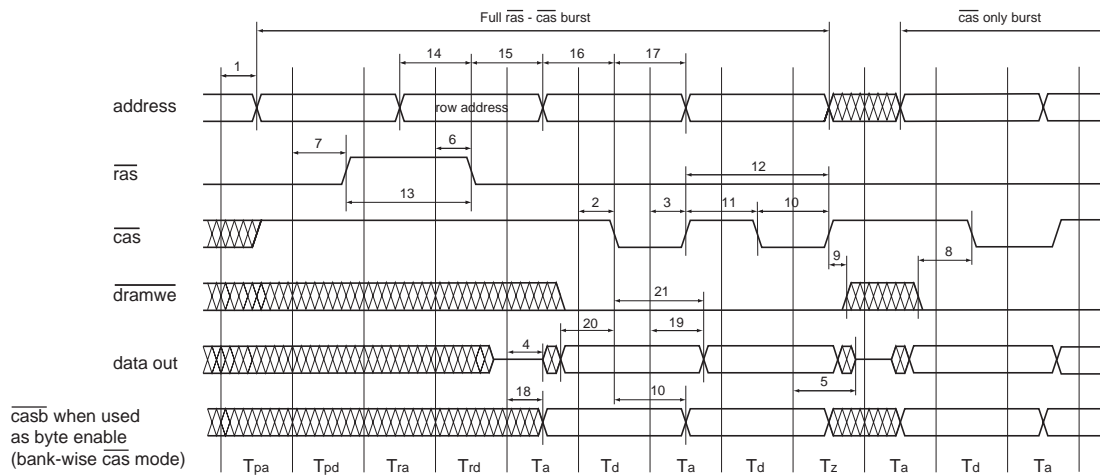


Figure 19-11 Asynchronous DRAM - Write Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock.	2	-	8	-	ns
2	t_{casl}	\overline{cas} low delay from clock.	2	-	8	5-c	ns
3	t_{cash}	\overline{cas} high delay from clock.	2	-	8	-	ns
4	t_{doe}	Data out turn on time from clock.	7	-	-	-	ns
5	t_{doz}	Data out turn off time from clock.	-	-	10	10-cz	ns
6	t_{rasl}	\overline{ras} low time from clock.	3	-	10	-	ns
7	t_{rash}	\overline{ras} high time from clock.	8	-	13	-	ns
8	t_{wcs}	\overline{dramwe} low setup time to \overline{cas} low.	2	-	-	-	ns
9	t_{weh}	\overline{dramwe} low hold time from \overline{cas} high.	1	-	-	-	ns
10	t_{cas}	\overline{cas} pulse width.	7	-	-	10-cw - 5-c	ns
11	t_{cp}	\overline{cas} precharge time.	7	-	-	10-cp + 5-c	ns
12	t_{pc}	\overline{cas} cycle time.	-	20	-	10·(cp + cw)	ns
13	t_{rp}	\overline{ras} precharge time.	14	-	-	10·(rp + rs)	ns
14	t_{asr}	Row address setup time to \overline{ras} .	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from \overline{ras} .	4	-	12	10-rh	ns
16	t_{asc}	Column address setup time to \overline{cas} .	7	-	-	10-cp + 5-c	ns
17	t_{cah}	Column address hold time from \overline{cas} .	7	-	-	10-cw - 5-c	ns
18	t_{be}	\overline{casb} delay from clock, when used as byte enable (bankwise mode).	2	-	8	-	ns
19	t_{do}	Data delay from clock.	6	-	-	-	ns
20	t_{dsc}	Data setup to \overline{cas} low.	2	-	-	5-c	ns
21	t_{dhc}	Data hold after \overline{cas} low.	10	-	-	10-cw - 5-c	ns

Table 19-58 Asynchronous DRAM - Write Timing

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

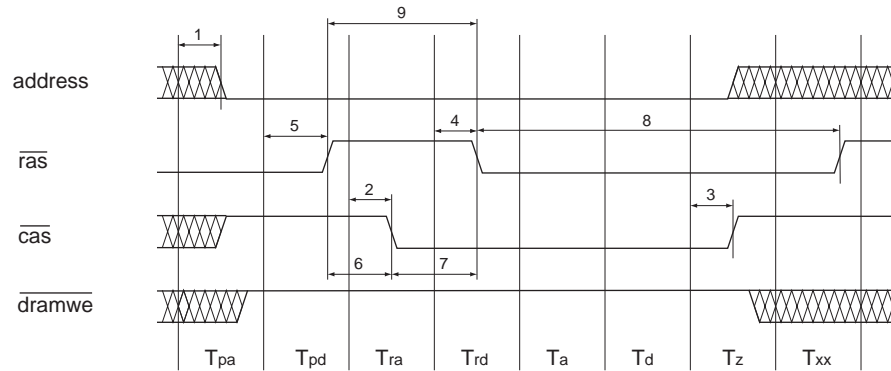


Figure 19-12 $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock.	2	-	8	-	ns
2	t_{casl}	$\overline{\text{cas}}$ low delay from clock.	2	-	8	5-c	ns
3	t_{cash}	$\overline{\text{cas}}$ high delay from clock.	2	-	8	-	ns
4	t_{rasl}	$\overline{\text{ras}}$ low time from clock.	3	-	10	-	ns
5	t_{rash}	$\overline{\text{ras}}$ high time from clock.	8	-	13	-	ns
6	t_{rpc}	$\overline{\text{ras}}$ to $\overline{\text{cas}}$ precharge time.	2	-	-	10·rp	ns
7	t_{csr}	$\overline{\text{cas}}$ setup time to $\overline{\text{ras}}$.	7	-	-	10·rs	ns
8	t_{ras}	$\overline{\text{ras}}$ pulse width.	40	-	-	10·(rh + cp + cw)	ns
9	t_{rp}	$\overline{\text{ras}}$ precharge time.	14	-	-	10·(rp + rs)	ns

Table 19-59 $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle Timing

19.13.5 General Bus Interface Timing Diagrams

Data Turn-off Timing

This diagram specifies the relationships of the data turn-off timing of Asynchronous DRAM and non-DRAM bursts.

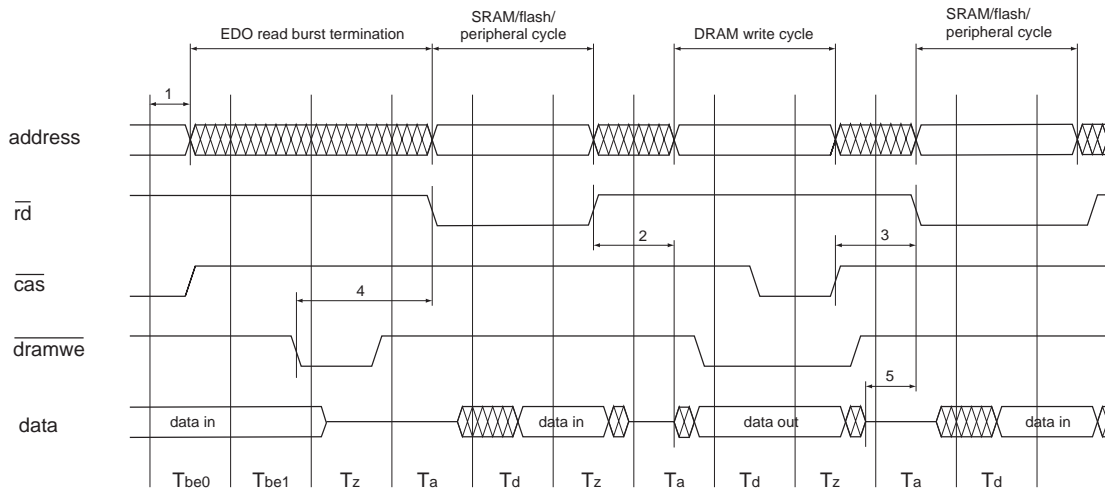


Figure 19-13 Data Turn-off Timing Diagram

No	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock.	2	-	8	-	ns
2	t_{rdo}	Read high to data out.	13	-	-	10-zw	ns
3	t_{cr}	\overline{cas} high to read low.	7	-	-	10-cz	ns
4	t_{welr}	\overline{dramwe} low to read low after EDO read burst.	13	-	-	10-cz	ns
5	t_{dozr}	Data out turn-off before read low.	5	-	-	-	ns

Table 19-60 Data Turn-off Timing

External Interrupt Acknowledge Cycle

The external interrupt acknowledge cycle always uses a maximum number of waitstates.

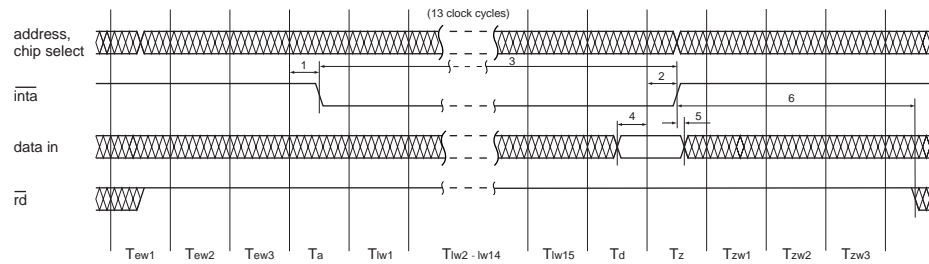


Figure 19-14 External Interrupt Acknowledge Cycle Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{il}	$\overline{\text{inta}}$ low delay from clock.	2	-	8	ns
2	t_{ih}	$\overline{\text{inta}}$ high delay from clock.	2	-	7	ns
3	t_{iw}	$\overline{\text{inta}}$ pulse width.	167	170	172	ns
4	t_{ds}	Data in setup time to clock.	0	-	-	ns
5	t_{dh}	Data in hold time from $\overline{\text{inta}}$ high.	0	-	-	ns
6	t_{ihr}	$\overline{\text{inta}}$ high to read low.	38	-	-	ns

Table 19-61 External Interrupt Acknowledge Cycle Timing

Timing of $\overline{\text{wait}}$ and $\overline{\text{rerun}}$

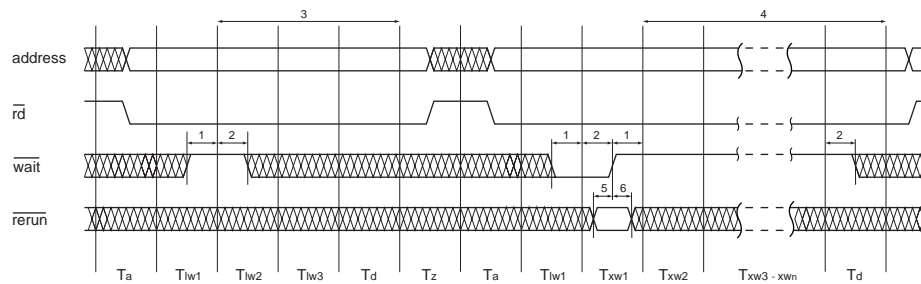


Figure 19-15 Wait and Rerun Timing Diagram

No	Name	Explanation	Min	Nom	Max	Note	Unit
1	t_{xws}	$\overline{\text{wait}}$ setup time to clock.	1	-	-	Note 11	ns
2	t_{xwh}	$\overline{\text{wait}}$ hold time from clock.	2	-	-	Note 11	ns
3	t_{xwi}	$\overline{\text{wait}}$ sampled to end of bus cycle ($\overline{\text{wait}}$ not activated).	30	30	30	Note 12	ns
4	t_{xwa}	$\overline{\text{wait}}$ sampled to end of bus cycle ($\overline{\text{wait}}$ activated).	50	-	80	Note 12	ns
5	t_{res}	$\overline{\text{rerun}}$ setup time to $\overline{\text{wait}}$ high.	1	-	-	-	ns
6	t_{reh}	$\overline{\text{rerun}}$ hold time after $\overline{\text{wait}}$ high.	1	-	-	-	ns

Table 19-62 Wait and Rerun Timing

Note 11: The $\overline{\text{wait}}$ signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

Note 12: The $\overline{\text{wait}}$ signal is sampled three clock cycles before the end of the bus cycle, taking only the internal wait states into consideration. To recognize $\overline{\text{wait}}$, a number of internal lw and/or ew waitstates must be added. Typically, three internal wait states are necessary, but this depends on the external wait state logic.

19.13.6 External DMA Timing Diagrams

External DMA, Handshake Mode Timing, Read

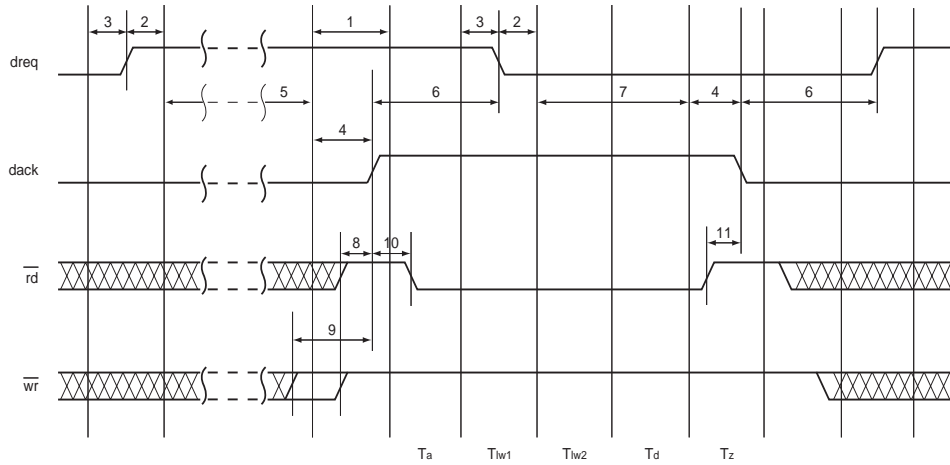


Figure 19-16 External DMA, Handshake Mode Timing, Read

The timing diagram above is shown with **dreq** and **dack** configured to be active high, and with two late waitstates (The number of waitstates is just an example however; there does not need to be two waitstates.).

Number	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_{ckp}	Internal clock period	-	10	-	-	ns
2	t_{drs}	dreq setup time to clock (note 13)	1	-	-	-	ns
3	t_{drh}	dreq hold time from clock (note 13)	2	-	-	-	ns
4	t_{dack}	dack delay from clock	8	-	17	-	ns
5	t_{drda}	dreq to dack latency	$4 * t_{ckp}$	-	-	-	ns
6	t_{dadr}	dreq hold time from dack	0	-	-	-	ns
7	t_{dai}	dreq inactive to dack inactive latency (note 14)	$2 * t_{ckp}$	-	-	-	ns
8	t_{rwda}	\overline{wr} (extended write) high or \overline{rd} high to dack active	5	-	-	-	ns
9	t_{wrda}	\overline{wr} (normal write) high to dack active	10	-	-	-	ns
10	t_{dard}	dack active to \overline{rd} low	1	-	-	$10 * \max(0, ew - 1)$	ns
11	t_{rhda}	\overline{rd} high to dack inactive	5	-	-	-	ns

Table 19-63 External DMA, Handshake Mode Timing, Read

Note 13: The **dreq** signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

Note 14: t_{dai} will be the maximum of $2 * t_{ckp}$ and the time to the end of the Td state of the external DMA bus cycle.

External DMA, Handshake Mode Timing, Write

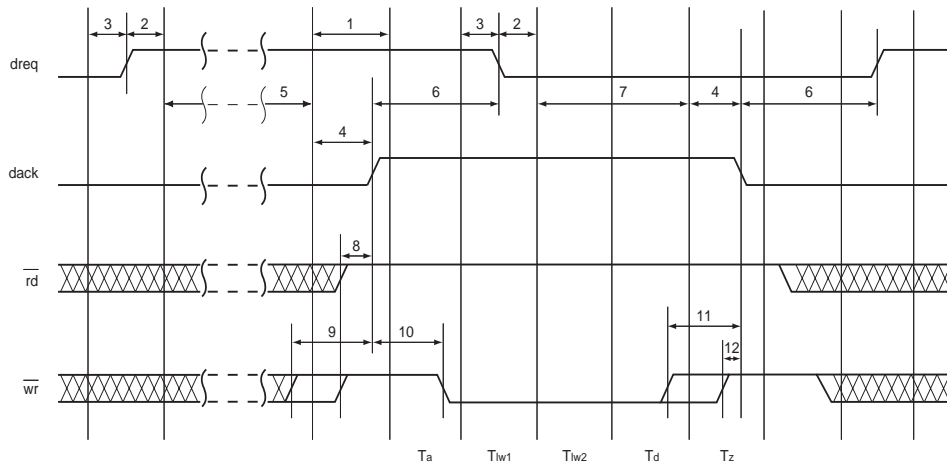


Figure 19-17 External DMA, Handshake Mode Timing, Write

The timing diagram above is shown with **dreq** and **dack** configured to be active high, and with two late waitstates (The number of waitstates is just an example however; there does not need to be two waitstates.).

Number	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_{ckp}	Internal clock period	-	10	-	-	ns
2	t_{drs}	dreq setup time to clock (note 15)	1	-	-	-	ns
3	t_{drh}	dreq hold time from clock (note 15)	2	-	-	-	ns
4	t_{dack}	dack delay from clock	8	-	17	-	ns
5	t_{drda}	dreq to dack latency	$4 * t_{ckp}$	-	-	-	ns
6	t_{dadr}	dreq hold time from dack	0	-	-	-	ns
7	t_{dai}	dreq inactive to dack inactive latency (note 16)	$2 * t_{ckp}$	-	-	-	ns
8	t_{rwda}	\overline{wr} (extended write) high or \overline{rd} high to dack active	5	-	-	-	ns
9	t_{wrda}	\overline{wr} (normal write) high to dack active	10	-	-	-	ns
10	t_{dawr}	dack active to \overline{wr} low	6	-	-	$10 * \max(0, ew - 1)$	ns
11	t_{whda}	\overline{wr} (normal write) high to dack inactive	10	-	-	-	ns
12	t_{weda}	\overline{wr} (extended write) high to dack inactive	5	-	-	-	ns

Table 19-64 External DMA, Handshake Mode Timing, Write

Note 15: The **dreq** signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

Note 16: t_{dai} will be the maximum of $2 * t_{ckp}$ and the time to the end of the Td state of the external DMA bus cycle.

External DMA, Burst Mode Timing, Read

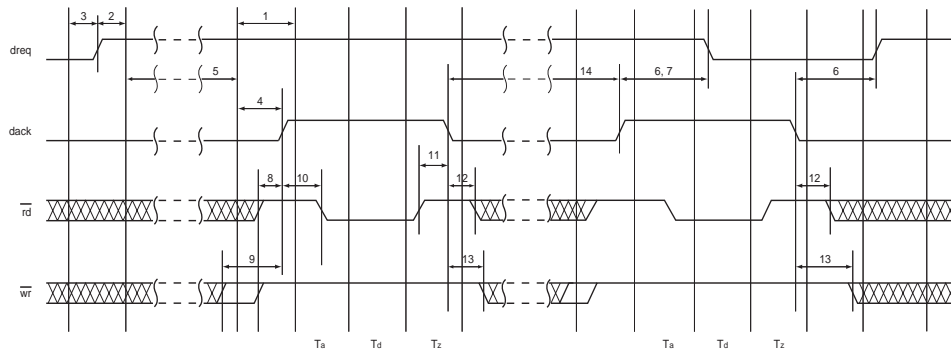


Figure 19-18 External DMA, Burst Mode Timing, Read

The timing diagram above is shown with **dreq** and **dack** configured to be active high, and with 0 waitstates.

Number	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_{ckp}	Internal clock period	-	10	-	-	ns
2	t_{drs}	dreq setup time to clock (note 17)	1	-	-	-	ns
3	t_{drh}	dreq hold time from clock (note 17)	2	-	-	-	ns
4	t_{dack}	dack delay from clock	8	-	17	-	ns
5	t_{drda}	dreq to dack latency	$4 * t_{ckp}$	-	-	-	ns
6	t_{dadr}	dreq hold time from dack	0	-	-	-	ns
7	t_{dadi}	dreq inactive time from dack	-	-	12	$10 * (\max(0, ew - 1) + lw)$	ns
8	t_{rwda}	\overline{wr} (extended write) high or \overline{rd} high to dack active	5	-	-	-	ns
9	t_{wrda}	\overline{wr} (normal write) high to dack active	10	-	-	-	ns
10	t_{dard}	dack active to \overline{rd} low	1	-	-	$10 * \max(0, ew - 1)$	ns
11	t_{rhda}	\overline{rd} high to dack inactive	5	-	-	-	ns
12	t_{dair}	dack inactive to \overline{rd} low	1	-	-	$10 * zw$	ns
13	t_{daiw}	dack inactive to \overline{wr} low	6	-	-	$10 * zw$	ns
14	t_{dada}	dack inactive to dack active time	17	-	-	-	ns

Table 19-65 External DMA, Burst Mode Timing, Read

Note 17: The **dreq** signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

External DMA, Burst Mode Timing, Write

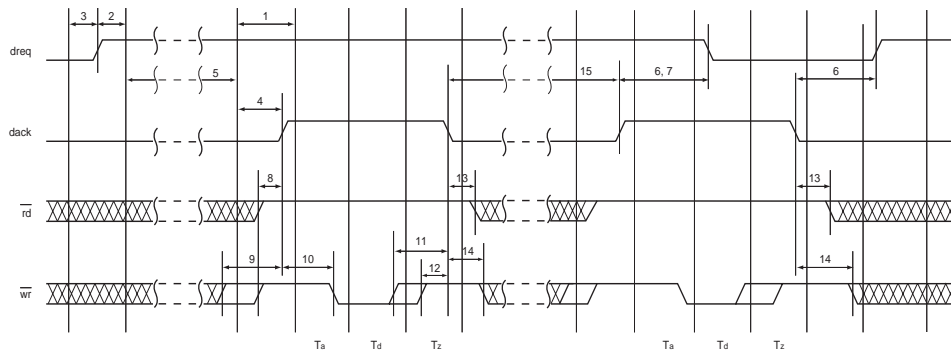


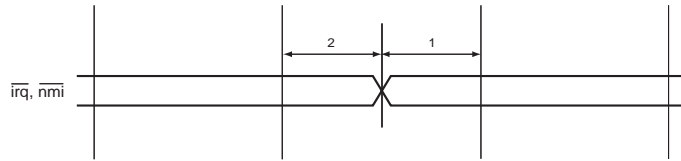
Figure 19-19 External DMA, Burst Mode Timing, Write

The timing diagram above is shown with **dreq** and **dack** configured to be active high, and with 0 waitstates.

Number	Name	Explanation	Without Waitstates			Add with Waitstates	Unit
			Min	Nom	Max		
1	t_{ckp}	Internal clock period	-	10	-	-	ns
2	t_{drs}	dreq setup time to clock (note 18)	1	-	-	-	ns
3	t_{drh}	dreq hold time from clock (note 18)	2	-	-	-	ns
4	t_{dack}	dack delay from clock	8	-	17	-	ns
5	t_{drda}	dreq to dack latency	$4 \cdot t_{ckp}$	-	-	-	ns
6	t_{dadr}	dreq hold time from dack	0	-	-	-	ns
7	t_{dadi}	dreq inactive time from dack	-	-	12	$10 \cdot (\max(0, ew-1) + lw)$	ns
8	t_{rwda}	\overline{wr} (extended write) high or \overline{rd} high to dack active	5	-	-	-	ns
9	t_{wrda}	\overline{wr} (normal write) high to dack active	10	-	-	-	ns
10	t_{dawr}	dack active to \overline{wr} low	6	-	-	$10 \cdot \max(0, ew-1)$	ns
11	t_{whda}	\overline{wr} (normal write) high to dack inactive	10	-	-	-	ns
12	t_{weda}	\overline{wr} (extended write) high to dack inactive	5	-	-	-	ns
13	t_{dair}	dack inactive to \overline{rd} low	1	-	-	$10 \cdot zw$	ns
14	t_{daiw}	dack inactive to \overline{wr} low	6	-	-	$10 \cdot zw$	ns
15	t_{dada}	dack inactive to dack active time	17	-	-	-	ns

Table 19-66 External DMA, Burst Mode Timing, Write

Note 18: The **dreq** signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

19.13.7 $\overline{\text{irq}}$ and $\overline{\text{nmi}}$ TimingFigure 19-20 $\overline{\text{irq}}$ and $\overline{\text{nmi}}$ Timing

Number	Name	Explanation	Min	Nom	Max	Unit
1	t_{irqs}	$\overline{\text{irq}}$ and $\overline{\text{nmi}}$ setup time to clock (note 19)	6	-	-	ns
2	t_{irqh}	$\overline{\text{irq}}$ and $\overline{\text{nmi}}$ hold time from clock (note 19)	-3	-	-	ns

Table 19-67 $\overline{\text{irq}}$ and $\overline{\text{nmi}}$ Timing

Note 19: The $\overline{\text{irq}}$ and $\overline{\text{nmi}}$ signals are synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

19.13.8 Shared RAM Interface Timing

Shared RAM Interface, Peripheral Read and Write Cycle Timing

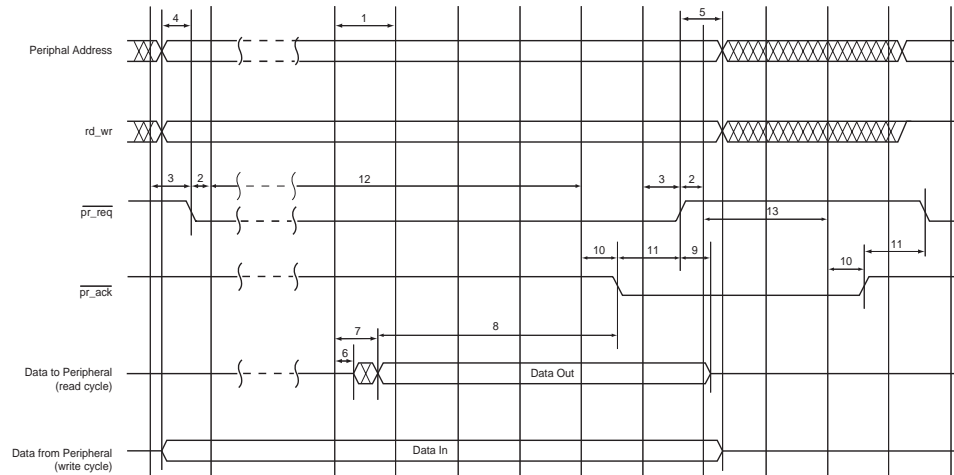


Figure 19-21 Shared RAM Interface, Peripheral Read and Write Cycle Timing

Number	Name	Explanation	Min	Nom	Max	Unit
1	t_{ckp}	Internal clock period	-	10	-	ns
2	t_{srqs}	$\overline{pr_req}$ setup time to clock (note 20)	2	-	-	ns
3	t_{srqh}	$\overline{pr_req}$ hold time from clock (note 20)	1	-	-	ns
4	t_{srs}	Peripheral address, peripheral data and rd_wr setup time to $\overline{pr_req}$	0	-	-	ns
5	t_{srh}	Peripheral address, peripheral data and rd_wr hold time from $\overline{pr_req}$	0	-	-	ns
6	t_{stroe}	Data output enable time from clock	7	-	-	ns
7	t_{srdv}	Data to peripheral valid from clock	-	-	17	ns
8	t_{srdv}	Data to peripheral setup time to $\overline{pr_ack}$	27	-	-	ns
9	t_{srdh}	Data to peripheral hold time from $\overline{pr_req}$	1	-	-	ns
10	t_{srad}	$\overline{pr_ack}$ delay from clock	3	-	12	ns
11	t_{srap}	$\overline{pr_req}$ delay from $\overline{pr_ack}$	0	-	-	ns
12	t_{srra}	$\overline{pr_req}$ to $\overline{pr_ack}$ latency	$12 \cdot t_{ckp}$	-	-	ns
13	t_{srrl}	$\overline{pr_req}$ inactive to $\overline{pr_ack}$ inactive latency	$2 \cdot t_{ckp}$	$2 \cdot t_{ckp}$	$2 \cdot t_{ckp}$	ns

Table 19-68 Shared RAM Interface, Peripheral Read and Write Cycle Timing

Note 20: The $\overline{pr_req}$ signal is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

Shared RAM Interface, a_sel Timing

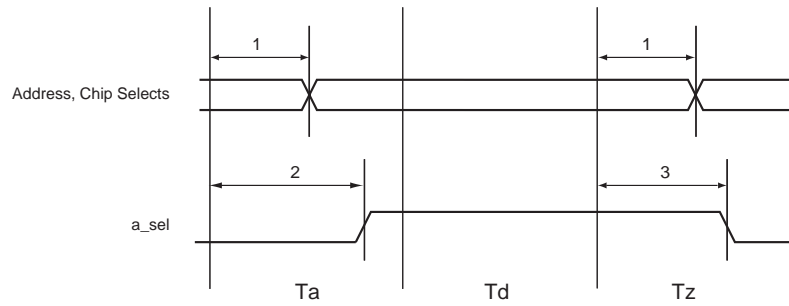


Figure 19-22 Shared RAM Interface, a_sel Timing

Number	Name	Explanation	Min	Nom	Max	Unit
1	t_a	Address and chip select delay from clock	2	-	8	ns
2	t_{srsh}	a_sel high delay from clock	3	-	10	ns
3	t_{srsl}	a_sel low delay from clock	3	-	11	ns

Table 19-69 Shared RAM Interface, a_sel Timing

Shared RAM Interface, Interrupt Timing

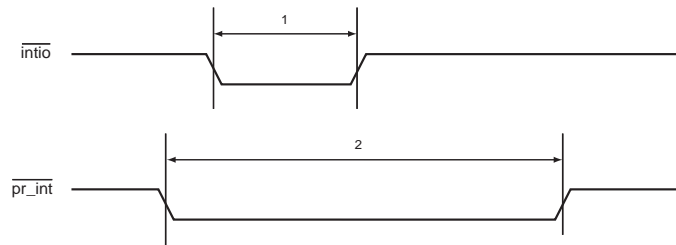


Figure 19-23 Shared RAM Interface, Interrupt Timing

Number	Name	Explanation	Min	Nom	Max	Unit
1	t_{sriw}	$\overline{\text{intio}}$ pulse width	25	-	-	ns
2	t_{srpw}	$\overline{\text{pr_int}}$ pulse width	590	600	610	ns

Table 19-70 Shared RAM Interface, Interrupt Timing

19.13.9 Network Interface Timing

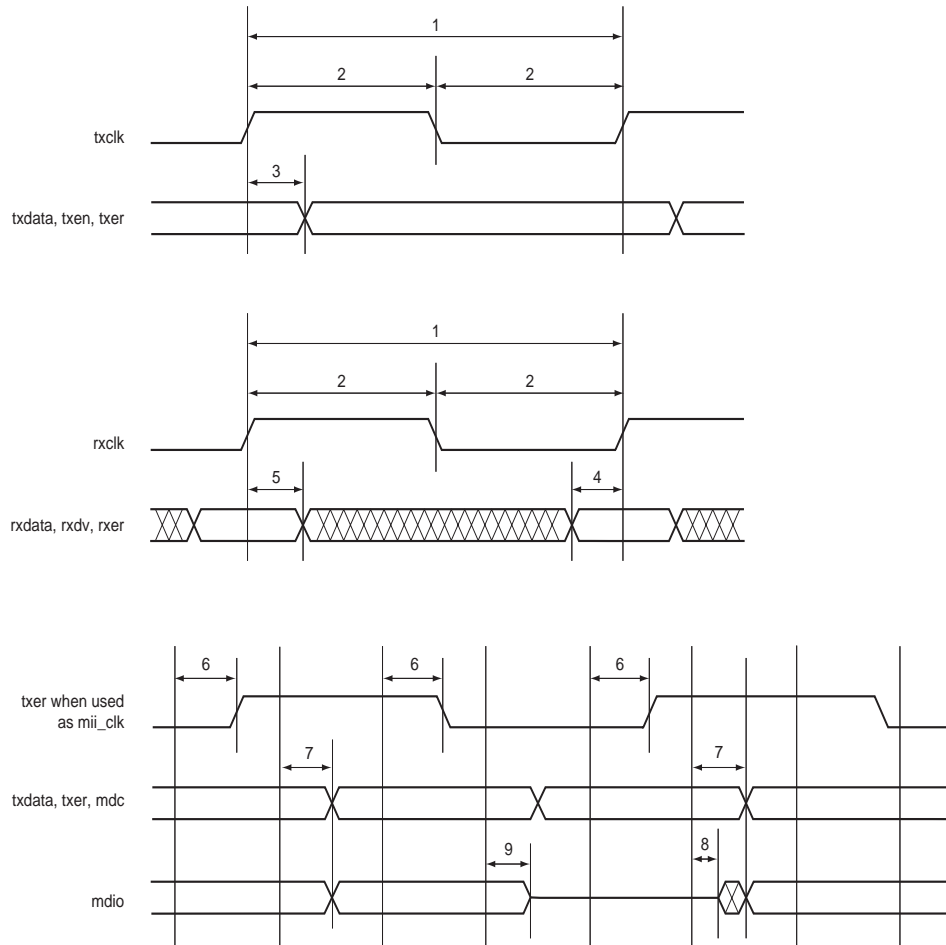


Figure 19-24 Network Interface Timing

Number	Name	Explanation	Min	Nom	Max	Unit
1	t_{etcp}	txclk and rxclk clock period, MII operation txclk and rxclk clock period, SNI operation	35 70	- -	- -	ns ns
2	t_{etcw}	txclk and rxclk pulse width	10	-	-	ns
3	t_{etdd}	txdata , txen and txer delay from txclk	4	-	16	ns
4	t_{etds}	rxdata , rxdv and rxer setup time to rxclk	3	-	-	ns
5	t_{etdh}	rxdata , rxdv and rxer hold time from rxclk	1	-	-	ns
6	t_{etcd}	txer delay from internal clock, when used as 25MHz clock output	7	-	16	ns
7	t_{etmd}	txdata , txer , mdc and mdio delay from internal clock, when controlled by the R_NETWORK_MGM_CTRL mode register	7	-	15	ns
8	t_{etme}	mdio output enable from internal clock	6	-	-	ns
9	t_{etmz}	mdio turn off time from internal clock	6	-	14	ns

Table 19-71 Network Interface Timing

19.13.10 Reset and Clock Timing

System Clock Timing

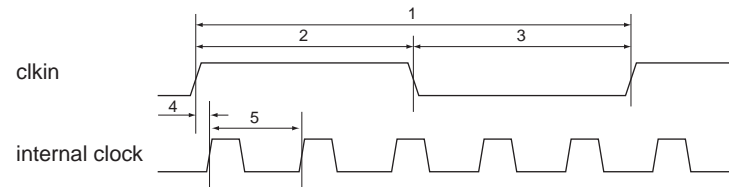


Figure 19-25 System Clock Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{clkp}	Input clock period (Note 21).	49	50	51	ns
2	t_{clkh}	Input clock high time.	15	-	-	ns
3	t_{clkl}	Input clock low time.	15	-	-	ns
4	t_{clkd}	Input clock to internal clock delay.	0.9	2.5	4	ns
5	t_{ckp}	Internal clock period.	-	$0.2 \cdot t_{clkp}$	-	ns

Table 19-72 System Clock Timing

Note 21: Some applications may require less tolerance on the clock period. For example, if txer is configured as the clock for Fast Ethernet, greater clock cycle accuracy is needed (see 100BASE-T standard: IEEE 802.3u.).

Reset Timing

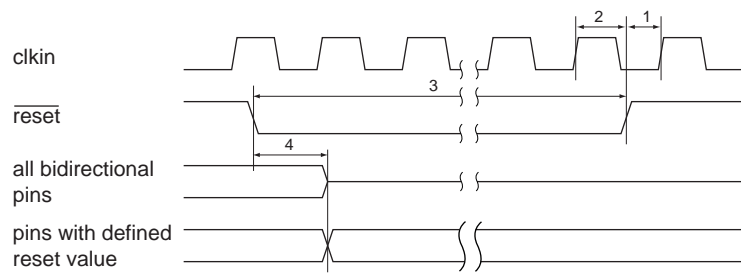


Figure 19-26 Reset Timing Diagram

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{ress}	$\overline{\text{reset}}$ setup to clkln. (Note 22).	2	-	-	ns
2	t_{resh}	$\overline{\text{reset}}$ hold from clkln. (Note 22).	1	-	-	ns
3	t_{resw}	$\overline{\text{reset}}$ pulse width.	$5 \cdot t_{\text{clkp}}$	-	-	ns
4	t_{resd}	$\overline{\text{reset}}$ to output delay.	-	-	25	ns

Table 19-73 Reset Timing

Note 22: The $\overline{\text{reset}}$ signal is internally synchronized. Setup and hold times can be ignored unless recognition on a specific clock cycle is required.

19.14 Physical Dimensions

The package of the ETRAX 100LX is a 256 lead Plastic Ball Grid Array (PBGA).

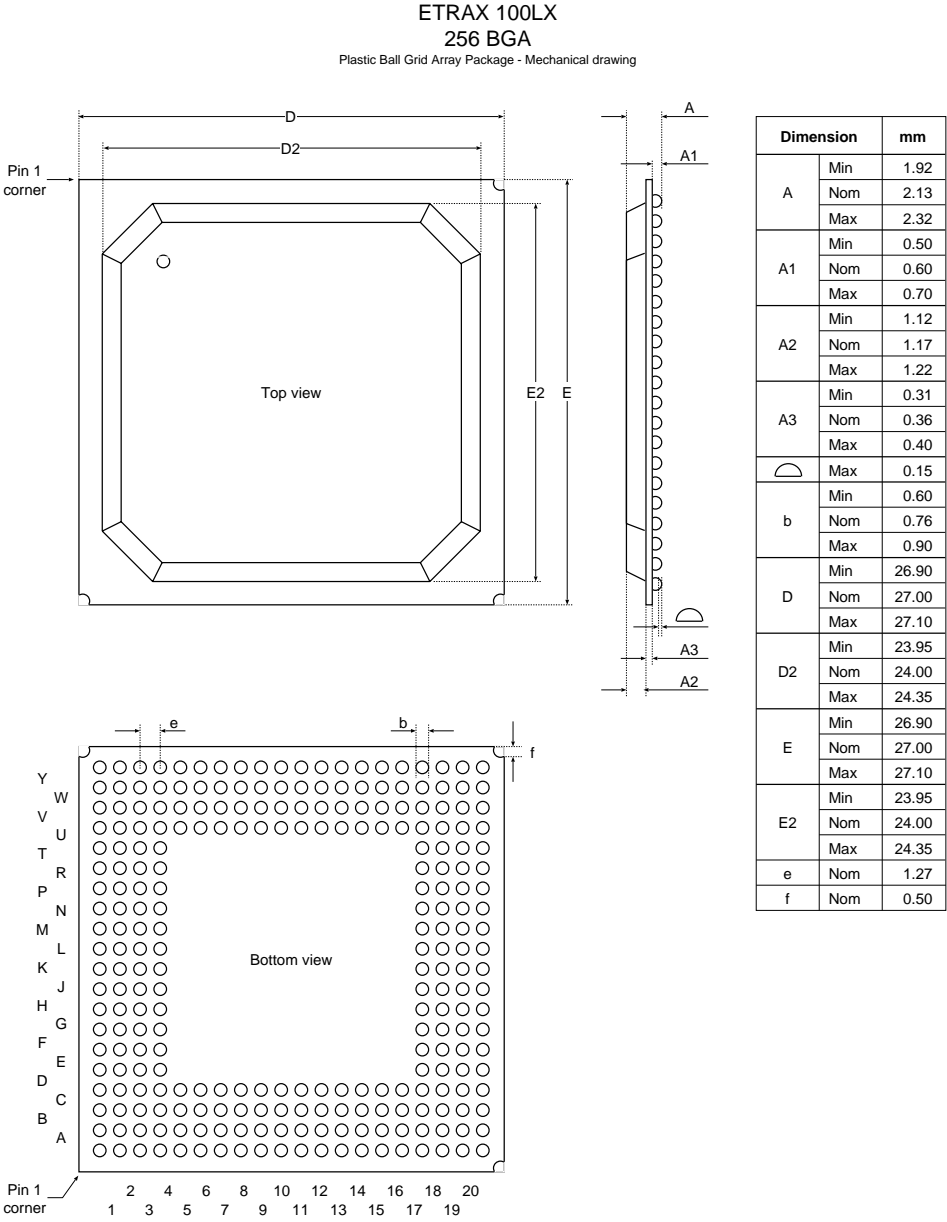


Figure 19-27 256 PBGA - Mechanical Drawing

