1 Introduction

Optimized Network Controller with
RISC CPU, Cache
and Multiple I/O Ports

1.1 Overview

The AXIS ETRAX 100LX is a single-chip integrated circuit designed for embedded network connectivity applications. The ETRAX 100LX improves upon the features available for the AXIS ETRAX 100, including support for Universal Serial Bus 1.1. It is compatible with the widespread ETRAX family, and offers further advances in microprocessor design and performance. The ETRAX 100LX chip incorporates the AXIS CRIS CPU which not only suits all the requirements of a network connectivity product, but also acts as an integrated core especially suited for our system.

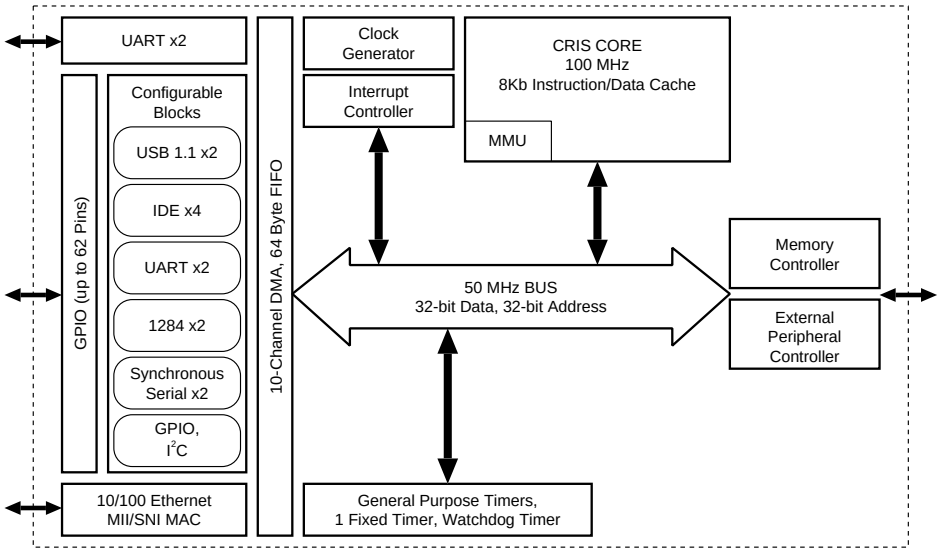
The ETRAX 100LX is ideal in executing multi protocol network stacks on one chip. The ETRAX 100LX has a 100 MIPS RISC CPU, 8 kilobyte unified instruction/data cache, high bandwidth DMA controlled I/O ports, and an on-chip Fast Ethernet controller. Its integrated functions, minimal power consumption, and high code density makes it highly suitable for a wide range of embedded applications that require high performance and low system cost.

The ETRAX 100LX programmable bus interface supports both 16-bit and 32-bit data bus widths, and interfaces directly to SDRAM, EDO DRAM, SRAM, EPROM, parallel EEPROM, and FlashPROM.

1.2 Features

- High performance 100 MIPS (200 MIPS/W) 32-bit RISC CPU, 112k Dhrystones.
- Designed specifically for running Linux by including an MMU.
- Ethernet controller supports 100Mbit/10Mbit MII (Compatible with IEEE 802.3 and Fast Ethernet standards).
- Four asynchronous serial ports with an internal baudrate programmable from 48 Hz to 6.25 MHz, and an external baudrate up to 3.125 MHz.
- Two synchronous serial ports. Master or Slave synchronous serial mode with a codec clock between 32 kHz and 4.096 MHz.
- Universal Serial Bus 1.1 Host and Device mode operation. Hardware support for dynamic connect/disconnect, suspend/resume and remote wakeup.
- Configuration of up to four EIDE/ATA-2 ports for up to 8 IDE disk drives.
- 16-bit general I/O port. The direction of each bit can be individually controlled.
- Two configurable parallel I/O ports for Centronics, IEEE 1284 byte, ECP, and EPP mode, and Shared RAM interface.
- Optimized for compact code and high speed with configurable 16-bit or 32-bit bus width.
- Bus interface supporting SDRAM, EDO DRAM, SRAM, EPROM, parallel EEPROM, and FlashPROM.
- 8 kilobyte on chip cache memory.
- DMA controlled network and port I/O for high performance
- Excellent C/C++ language support and high code density.
- Configurable bootstrap through network, serial, and parallel ports as well as FlashPROM.
- Low power consumption, 350 mW typically.
- 256-pin PBGA package, 27 x 27 x 2.15 mm.

1.3 Functional Block Diagram



The CPU in ETRAX 100LX is a RISC CPU with internal cache memory. Data handling is provided by internal DMA within the chip as well as to and from external units. The internal clocks are generated by a PLL clock multiplier that takes its input from an external clock generator. ETRAX 100LX provides internal and external vectorized interrupt.