

7 The ETRAX 4

7.1 Introduction

The ETRAX 4 is an earlier processor in the ETRAX family. The differences between the CRIS implementation in the ETRAX 100LX and the ETRAX 4 are presented in this chapter.

7.2 Special Registers

The processor architecture defines 16 *special registers* (P0 - P15), ten of which are implemented in the ETRAX 4. The special registers in the ETRAX 4 are:

MNEM	Reg.No.	Description	Width
VR	P1	Version register	8 bits
CCR	P5	Condition Code Register	16 bits
DCR0	P6	DMA Channel 0 Count Register	16 bits
DCR1	P7	DMA Channel 1 Count Register	16 bits
IBR	P9	Interrupt Base Register	32 bits
IRP	P10	Interrupt Return Pointer	32 bits
SRP	P11	Subroutine Return Pointer	32 bits
DTP0	P12	DMA Channel 0 Transfer Pointer	32 bits
DTP1	P13	DMA Channel 1 Transfer Pointer	32 bits
BRP	P14	Breakpoint Return Pointer	32 bits

Table 7-1 *Special Registers*

Special Registers for the ETRAX 4:

Figure 7-1 *Special Registers*

7.3 Flags and Condition Codes

The ETRAX 4 condition code register (CCR) has no F, P, U, M or B flags. Instead of the M and B flags, the ETRAX 4 has a D and E flag:

Figure 7-2 The ETRAX 4 Condition Code Register (CCR)

The DCCR register is not available in the ETRAX 4 (this affects the MOVE (to Pd) and POP (to Pd) instructions).

The only difference in the 16 condition codes in 7-2 below is the EXT (external pin); all other condition codes are the same.

Code	Alt	Condition	Encoding	Boolean Function
CC	HS	Carry Clear	0000	\overline{C}
CS	LO	Carry Set	0001	C
NE		Not Equal	0010	\overline{Z}
EQ		Equal	0011	Z
VC		Overflow Clear	0100	\overline{V}
VS		Overflow Set	0101	V
PL		Plus	0110	\overline{N}
MI		Minus	0111	N
LS		Low or Same	1000	C + Z
HI		High	1001	$\overline{C} * \overline{Z}$
GE		Greater or Equal	1010	$N * V + \overline{N} * \overline{V}$
LT		Less Than	1011	$N * \overline{V} + \overline{N} * V$
GT		Greater Than	1100	$N * V * \overline{Z} + \overline{N} * \overline{V} * \overline{Z}$
LE		Less or Equal	1101	$Z + N * \overline{V} + \overline{N} * V$
A		Always True	1110	1
EXT		External Pin	1111	External input

Table 7-2 The ETRAX 4 Condition Codes

This is the order in which the flags are listed in chapter section 2 *Instruction Set Description* (see section 3 *Instructions in Alphabetical Order*):

ETRAX 100LX: F P U M B I X N Z V C

ETRAX 4: - - - D E I X N Z V C

Except for there being no F, P or U flags in the instruction set for the ETRAX 4, and that the M and B flags are flags D and E respectively, the list of what flags are affected in the ETRAX 4 is the same except for the instructions in the table below:

Instruction		Flags Affected	
		D	E
CLEARF		*	*
MOVE to Pd	(Pd != CCR)	-	-
	(Pd == CCR)	-	-
POP		-	-

Table 7-3 Changes in Affected Flags for the ETRAX 4

7.4 Data Organization in Memory

The ETRAX 4 CPU can operate with an 8-bit or 16-bit wide data bus. Figure 7-3 shows an example of data organization with an 8-bit bus. The same example, but with a 16-bit bus, is shown in 7-4.

Example of a structure layout:

```
struct example
{
    byte  a;
    byte  b;
    word  c;
    dword d;
    byte  e;
    word  f;
    dword g;
};
```

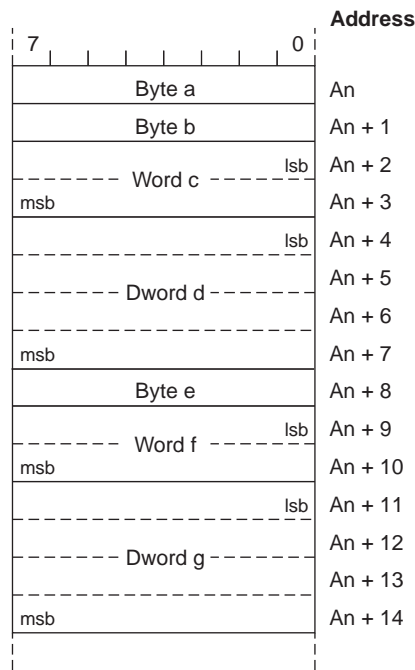


Figure 7-3 Data Organization with an 8-bit Bus

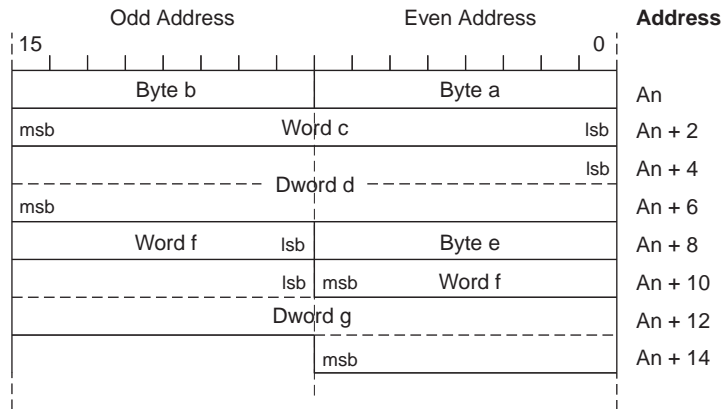


Figure 7-4 Data Organization with a 16-bit Bus

When a word or a dword is placed at odd addresses in a 16-bit memory (like word f and dword g in figure 7-4), each access to the data will require extra bus cycles. For maximum performance in 16-bit systems, it is recommended to keep word and dword data aligned to even addresses as much as possible.

7.5 Branches, Jumps and Subroutines

The EXT condition is not available in the ETRAX 100LX (see 7-2).

7.6 Interrupts and Breakpoints in the ETRAX 4

Only bits 29 and 30 of the Interrupt Base Register (IBR) are implemented in the ETRAX 4, the remaining bits are always zero.

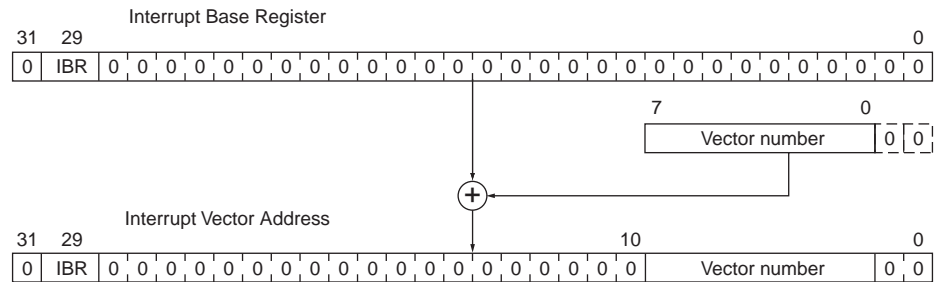


Figure 7-5 Interrupt Vector Address Calculation in the ETRAX 4

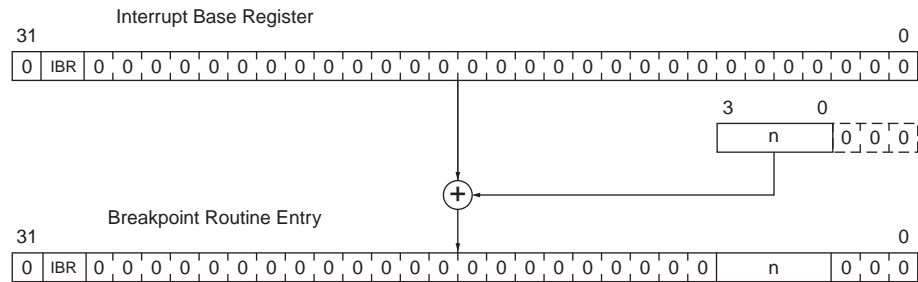


Figure 7-6 Software Breakpoint Address Calculation in the ETRAX 4

Hardware breakpoints are not implemented in the ETRAX 4.

7.7 Reset in the ETRAX 4

7.7.1 ROM Boot

After reset, the ETRAX 4 CPU starts the execution at address 00000002. The following registers are initialized after reset:

Register	Value (hex)
VR	3
CCR	0000
DCR0	1000
IBR	00000000
DTP0	00000002

Table 7-4 Initialization Values of Registers After Reset in the ETRAX 4

All other registers have unknown values after reset.

7.7.2 Automatic Program Download

When the automatic program download (“flash-load”) is enabled, the initial values of DCR0 and DTP0 change. After the completion of the program download, the registers have the following values:

Register	Value (hex)
VR	3
CCR	0000
DCR0	0000
IBR	00000000
DTP0	40001002

Table 7-5 Initialization Values of Registers After Automatic Program Download in the ETRAX 4

After the automatic program download, the ETRAX 4 CPU starts to execute at address 40000002 (hex) instead of 00000002.

7.8 DMA

In the ETRAX 100LX, the DMA is not a part of the CPU but a separate module on the chip. In the ETRAX 4, however, the DMA is an integrated part of the CPU.

7.8.1 The ETRAX 4 DMA

The ETRAX 4 CPU contains two DMA channels. Each channel has a 32-bit *DMA Transfer Pointer* (DTP), a 16-bit *DMA Count Register* (DCR), and a DMA enable flag (*D* or *E*). The connection of each channel to a physical I/O channel is described in the *ETRAX Data Sheet*.

To start a DMA transfer, the DTP of the channel is loaded with the start address of the data block to be transferred, and the DCR of the channel is loaded with the number of transfers. (Loading the DCR with zero will give 65 536 transfers). The DMA enable flag of the channel is then set with the SETF instruction.

For each transfer, the DTP is incremented by one (byte transfer) or two (word transfers), and the DCR is decremented by one. When the DCR counts down to zero, the DMA enable flag is set to zero and the transfers stop.

The DMA can be stopped and started at any time by clearing the DMA enable flag. Note that the SETF and CLEARF instructions are the only instructions that will affect the D and E flags. When CCR is updated using the MOVE instruction, the D and E flags are left unchanged.

DMA channel 0 is designed to be able to automatically load a program (“flash-load”) to the system RAM after power up. This feature is enabled by keeping the external FLASH_ input low during reset. In this case, 4096 Bytes (1000 hex) are transferred

to the system RAM area with start at address 40000002 hex, before the CPU starts to execute.

7.9 Instruction Set

The ETRAX 4 CPU has a few less instructions than the ETRAX 100LX CPU. The instructions which are not available in the ETRAX 4 are:

BWF, JBRC, JIRC, JMPU, JSRC, MULS, MULU, RBF, SBFS, SWAP

7.9.1 Differences in the Instructions

The following instructions are different in the ETRAX 4 compared to the same instructions in the ETRAX 100LX:

MOVEM (from memory) Move to multiple registerspage page -56
from memory

MOVEM (to memory) Move from multiple registerspage page -57
to memory

In autoincrement addressing mode, the address ($si + 4 * \text{<number of loaded registers>}$) is loaded to the specified register. For the ETRAX 4 this also applies to the indexed with assign and offset with assign addressing modes. This is different from the ETRAX 100LX and from other instructions where the address is stored before the increment.

PUSH (from Ps) Push special register onto page -73
stack

The following size information applies to the ETRAX 4:

- Size is set according to the size of the pushed register:

Size:	11	Byte (Ps = VR)
	10	Word (Ps = CCR, DCR0 or DCR1)
	00	Dword (Ps = BRP, IBR, IRP, SRP, DTP0 or DTP1)

Table 7-6

CLEARF Clear flags page page -27

SETF Set flags page page -82

- The two most significant bits are D and E:



7.10 Execution Times for the ETRAX 4

7.10.1 Introduction

Instruction execution times for all CRIS instructions and addressing modes are given below in numbers of CPU cycles. With no wait states, each bus cycle requires two system clock cycles. One system clock cycle is added for each wait state.

7.10.2 Instruction Execution Times

This section gives the execution times for instructions with the four basic addressing modes: Quick immediate, Register, Indirect, and Autoincrement. Except for the following four special cases, the execution time is the same for all instructions with the same addressing mode and data size.

General Case:

Addressing mode	Data size	Data alignment	Execution time	
			16-bit bus	8-bit bus
Quick immediate	6-bit	N/A	1	2
Register	Any	N/A	1	2
Indirect, Autoinc.	Byte	Any	2	3
Indirect, Autoinc.	Word	Even address	2	4
Indirect, Autoinc.	Word	Odd address	3	4
Indirect, Autoinc.	Dword	Even address	3	6
Indirect, Autoinc.	Dword	Odd address	5	6

Table 7-7

Special Case 1: Bcc Instruction

Branch offset size	Execution time	
	16-bit bus	8-bit bus
Byte	1	2
Word	2	4

Table 7-8 *Bcc Instruction*

Special Case 2: Movem Instruction

Addressing mode	Data size	Data alignment	Execution time	
			16-bit bus	8-bit bus
Indirect, Autoinc.	Dword	Even address	$2n + 1$	$4n + 2$
Indirect, Autoinc.	Dword	Odd address	$4n + 1$	$4n + 2$

Table 7-9 *MOVEM Instruction*

(Where n is the number of registers moved.)

Special Case 3: PC Operand

One idle bus cycle is added to the execution times given above, if PC is used as the destination operand in any of the following instructions:

ABS	ADD	ADDQ	ADDS	ADDU	AND
ANDQ	ASR	ASRQ	BTSTQ	MOVEM	MOVEQ
MOVE (except from a special register)			MOVS	MOVU	OR
ORQ	POP	SUB	SUBQ	SUBS	SUBU
XOR					

One idle bus cycle is also added for the TEST.m PC instruction.

Special Case 4: Break Instruction

The BREAK instruction takes two cycles to execute on a 16-bit data bus, and three cycles on an 8-bit data bus.

7.10.3 Complex Addressing Modes Execution Times

Table 7-10 below gives the extra execution time required to calculate the effective address in complex addressing modes. The effective address calculation time is added to the Indirect/Autoincrement execution time given in section 7.10.2 *Instruction Execution Times* to give the total execution time of the instruction.

Addressing mode	Data alignment	Execution time	
		16-bit bus	8-bit bus
Indexed	N/A	1	2
Indexed with assigned	N/A	1	2
Immediate Byte offset	N/A	1	2
Indirect Byte offset	any	2	3
Word offset	even address	2	4
Word offset	odd address	3	4
Dword offset	even address	3	6
Dword offset	odd address	5	6
Immediate Byte offset with assign	N/A	1	2
Indirect Byte offset with assign	any	2	3
Word offset with assign	even address	2	4
Word offset with assign	odd address	3	4
Dword offset with assign	even address	3	6
Dword offset with assign	odd address	5	6
Double indirect	even address	3	6
Double indirect	odd address	5	6
Double indirect with autoincrement	even address	3	6
Double indirect with autoincrement	odd address	5	6
Absolute	N/A	3	6

Table 7-10

Note 1: Data alignment refers to the alignment of data involved in the effective address calculation.

7.10.4 Interrupt Acknowledge Execution Time

The interrupt acknowledge sequence, including the interrupt acknowledge cycle and the interrupt vector read following it, requires 3 bus cycles on a 16-bit bus, and 5 bus cycles on an 8-bit bus.

7.10.5 DMA Transfer Execution Time

Each DMA transfer requires one bus cycle.