

1 INTRODUCTION

Optimized Network Controller with
RISC CPU, Cache
and Multiple I/O Ports



1.1 OVERVIEW

The AXIS ETRAX 100 is a single-chip integrated circuit designed for embedded network connectivity applications. This is the fifth generation network micro controllers from Axis, compatible with the widespread ETRAX family, and it offers significant advances in microprocessor design and performance. The ETRAX 100 chip incorporates the AXIS CRIS CPU which not only suits all the requirements of a network connectivity product, but also acts as an integrated core especially suited for our system.

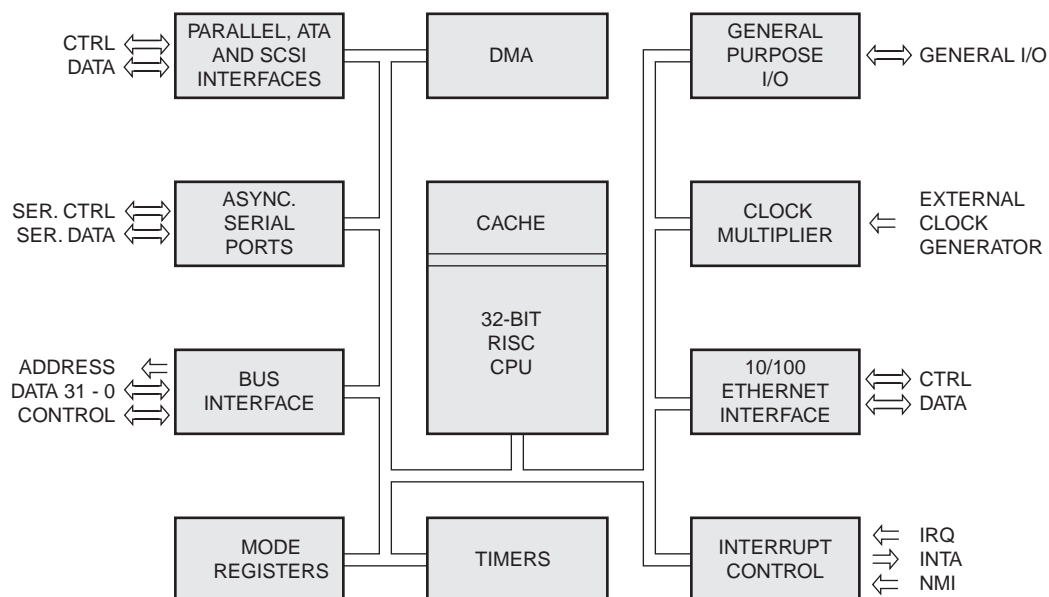
The ETRAX 100 is ideal in executing multi protocol network stacks on one chip. The ETRAX 100 has a 100 MIPS RISC CPU, 8 kilobyte unified instruction/data cache, high bandwidth DMA controlled I/O ports, and an on-chip Fast Ethernet controller. Its integrated functions, minimal power consumption, and high code density makes it highly suitable for a wide range of embedded applications that require high performance and low system cost, such as storage servers and web appliances.

The ETRAX 100 programmable bus interface supports both 16-bit and 32-bit data bus widths, and interfaces directly to SRAM, DRAM, EPROM, parallel EEPROM and flash memory without external logic.

1.2 FEATURES

- High performance 100 MIPS (200 MIPS/W) 32-bit RISC CPU, 112k Dhrystones.
- Ethernet controller supporting 100Mbit/10Mbit MII and 10 Mbit NS DP8391A compatible interface.
- Disk interface configurable as either EIDE/ATA-2, two 8-bit wide Ultra SCSI or one 16-bit wide Ultra SCSI interface.
- Two configurable parallel I/O ports for Centronics, HP Fast Mode, IBM/Lexmark FastByte, IEEE 1284 Bitronics ECP, and Shared RAM interface. These parallel I/O ports are multiplexed with the SCSI and EIDE/ATA-2 interfaces.
- Four serial ports with baud rate up to 1843.2 kbaud and a non standard baud rate of 6.25 Mbaud. Two dedicated serial ports and two ports multiplexed with SCSI and EIDE/ATA-2 interfaces.
- 16-bit general I/O port. The direction of each bit can be individually controlled.
- Configurable data bus width, 16-bit or 32-bit.
- Bus interface supporting SRAM, DRAM, EPROM, parallel EEPROM, and flash memory without external logic.
- 8 kilobyte on chip cache memory.
- DMA controlled network and port I/O for high performance
- Excellent C/C++ language support and high code density.
- Configurable bootstrap through network, serial, and parallel ports as well as PROM.
- Low power consumption, 500 mW typically.
- 256-pin PBGA package, 27 x 27 x 2.15 mm.

1.3 FUNCTIONAL BLOCK DIAGRAM



The CPU in ETRAX 100 is a RISC CPU with internal cache memory. Data handling is provided by internal DMA within the chip as well as to and from external units. The internal clocks are generated by a PLL clock multiplier that takes its input from an external clock generator. ETRAX 100 provides internal and external vectorized interrupt.

