3 BUS INTERFACE

The ETRAX 100 bus interface has a 32/16-bit data bus, a 25-bit address bus, and six internally decoded chip select outputs. Six additional chip select outputs are multiplexed with other I/O functions, and are available in some configurations. The bus interface also supports four DRAM banks without external logic.

3.1 DATA BUS

The 32-bit data bus provides support 16-bit wide memories. The data bus is organized with the least significant byte at the lowest address ("little endian").

The data bus 32-bit mode is shown in the figure below:

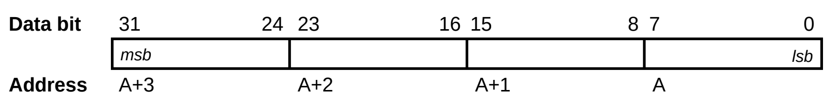

Figure 3-1 32-bit mode data bus

The data bus 16-bit mode is shown in the figure below:

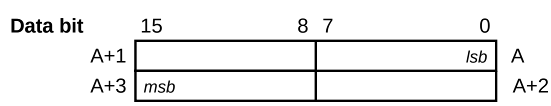

Figure 3-2 32-bit wide data on 16-bit mode data bus

3.2 ADDRESS AND CHIP SELECTS

The ETRAX 100 chip operates with a 32-bit wide address space internally, but only address bits 25-1 are available on the external pins. Address bits 30-26 are decoded internally to generate the different memory chip select outputs, and the select of DRAM banks and internal I/O. Address bit 31 is used to select whether the cache should be used or bypassed by CPU accesses.

The addresses are decoded to generate chip selects as follow:

Address range/Hex	Size /Mbyte	Name	Description
00000000-03FFFFFF	64	$\overline{CSE0}$	EPROM/flashPROM bank 0 chip select. See note 1.
04000000-07FFFFFF	64	$\overline{CSE1}$	EPROM/flashPROM bank 1 chip select. Note 1.
08000000-0BFFFFFF	64	$\overline{CSR0}$	SRAM bank 0 chip select. See note 1.
0C000000-0FFFFFFF	64	$\overline{CSR1}$	SRAM bank 1 chip select. See note 1.
10000000-13FFFFFF	64	$\overline{CSP0}$	Peripheral chip select 0. See note 1.
14000000-17FFFFFF	64	$\overline{CSP1}$	Peripheral chip select 1. See note 1, 2.
18000000-1BFFFFFF	64	$\overline{CSP2}$	Peripheral chip select 2. See note 1, 2.
1C000000-1FFFFFFF	64	$\overline{CSP3}$	Peripheral chip select 3. See note 1, 2.
20000000-23FFFFFF	64	$\overline{CSP4}$	Peripheral chip select 4. See note 1.
24000000-27FFFFFF	64	$\overline{CSP5}$	Peripheral chip select 5. See note 1, 2.
28000000-2BFFFFFF	64	$\overline{CSP6}$	Peripheral chip select 6. See note 1, 2.
2C000000-2FFFFFFF	64	$\overline{CSP7}$	Peripheral chip select 7. See note 1, 2.
30000000-3FFFFFFF	256	-	Do not use. See note 3.
40000000-7FFFFFFF	1024	-	DRAM interface. See note 1.
80000000-AFFFFFFF	768		Same as 00000000-2FFFFFFF but uncached.
B0000000-B7FFFFFF	128	-	Internal registers.
B8000000-BFFFFFFF	128	-	Internal start up code.
C0000000-FFFFFFFF	1024	-	Same as 40000000-7FFFFFFF but uncached.

Table 3-1

Note 1: Add 80000000 (hex) to bypass the cache.

Note 2: Peripheral select 1 - 3 and 5 - 7 are multiplexed with bits 2 - 7 in general port PB in the I/O block and are not available if these pins are configured as general port pins.

Note 3: This region is also internal registers and start-up code, but cached. Never use this area for accessing internal registers.

3.3 INTERNAL BUS ARBITRATION

The bus interface performs the bus arbitration between the possible internal bus masters. The bus priority order is:

1. Shared RAM interface *(highest priority)*
2. External DMA channels
3. DRAM refresh
4. Internal DMA channels
5. CPU and cache *(lowest priority)*

3.4 BUS WIDTH, CYCLE TIMING AND WAIT STATES

The bus interface supports 4 DRAM and 6 to 12 other memory banks depending on configuration, each connected to one of the chip select outputs. The banks are separated in five groups:

Group 1	$\overline{\text{CSE0}}$, $\overline{\text{CSE1}}$
Group 2	$\overline{\text{CSR0}}$, $\overline{\text{CSR1}}$
Group 3	$\overline{\text{CSP0}}$, $\overline{\text{CSP1}}$, $\overline{\text{CSP2}}$, $\overline{\text{CSP3}}$
Group 4	$\overline{\text{CSP4}}$, $\overline{\text{CSP5}}$, $\overline{\text{CSP6}}$, $\overline{\text{CSP7}}$
Group 5	DRAM banks

Table 3-2 Memory bank groups

The ETRAX 100 bus width and number of wait states can be configured individually for each group. The bus width can be configured to 16-bit or 32-bit. All banks in the same group have the same width. For group 1, the EPROM/flashPROM group, the initial bus width is decided by Bus Status pin 0 at hardware reset.

All bus cycles are run in consecutive bursts, with a maximum length of 32 bytes and a minimum length of 1 byte. A burst will never cross a 32-byte boundary. A burst is either read or write, the data direction is never changed within a burst.

For each group of banks, the following wait state parameters can be configured:

- Early wait states, ew, 2 bits
  Number of wait states before the falling edge of $\overline{\text{RD}}$, $\overline{\text{WR0}}$ - $\overline{\text{WR3}}$ or $\overline{\text{CAS}}$.
- Late wait states, lw, 4 bits (DRAM, 2 bits)
  Number of wait states after the falling edge of $\overline{\text{RD}}$, $\overline{\text{WR0}}$ - $\overline{\text{WR3}}$ or $\overline{\text{CAS}}$.
- Turn-off wait states, zw, 2 bits
  Number of wait states after the end of a burst. The turn-off wait states of the ending burst and the early wait states of the next burst may overlap.

	wait states range		
	Early	Late	Turn off
Group 1: $\overline{\text{CSE0}}$, $\overline{\text{CSE1}}$	0 – 3	0 – 15	0 – 3
Group 2: $\overline{\text{CSR0}}$, $\overline{\text{CSR1}}$	0 – 3	0 – 15	0 – 3
Group 3: $\overline{\text{CSP0}}$, $\overline{\text{CSP1}}$, $\overline{\text{CSP2}}$, $\overline{\text{CSP3}}$	0 – 3	0 – 15	0 – 3
Group 4: $\overline{\text{CSP4}}$, $\overline{\text{CSP5}}$, $\overline{\text{CSP6}}$, $\overline{\text{CSP7}}$	0 – 3	0 – 15	0 – 3
DRAM $\overline{\text{CAS}}$ cycle	0 – 3	0 – 3	0 – 3
DRAM $\overline{\text{RAS}}$ cycle	0 – 3	0 – 3	–
DRAM $\overline{\text{RAS}}$ precharge cycle	–	0 – 3	–

Table 3-3 Possible wait state settings

A zero waitstate bus cycle lasts 20 ns. Between bursts there are 10 ns. Each waitstate adds 10 ns to the bus cycle time. Default after reset is maximum number of wait states.

3.5 NORMAL AND EXTENDED WRITE MODE

During a normal ETRAX 100 write cycle, the $\overline{\text{WR0}}$ - $\overline{\text{WR3}}$ strobes will go high

5 ns before the end of the bus cycle. The write pulses can be extended to the end of the bus cycle. The write mode is individually configurable for each of the five groups of memory banks.

3.6 MEMORY TIMING

The timing for the read cycles, both with and without early wait states, is shown in the figure below. This timing diagram is valid for SRAM, flash and peripheral devices

.

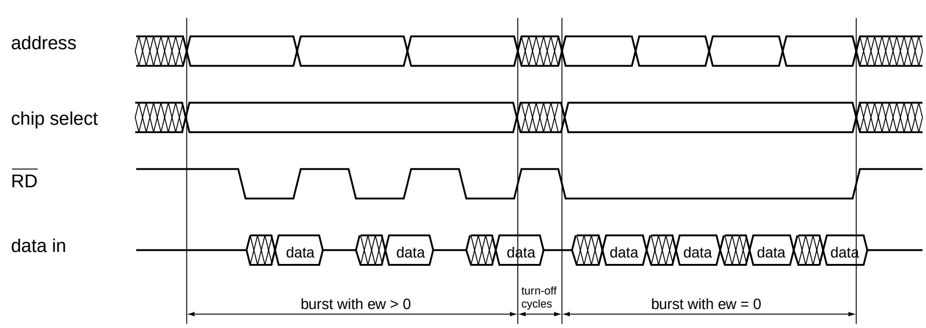

Figure 3-3 Read cycles for SRAM, flash memory and peripheral devices.

3.7 DRAM INTERFACE

The DRAM interface supports up to four banks of DRAM chips without external logic. 32-bit and 64-bit wide DRAM modules are supported as well as separate

DRAM chips. The DRAM bus width can be configured to 16 or 32 bits. Either Fast page mode or Hyper page mode (EDO) type DRAMs can be used. Maximum bus speed is 50 MHz.

All DRAM accesses are performed in bursts. When the first access in a series of bursts is performed, the internal address is shifted down, so that the row address appears on the lower pins of the address bus. The row address is stored in an internal register in ETRAX 100 for later reference. When the $\overline{\text{RAS}}$ portion of the cycle is finished, the column address is put on the address bus.

For every new burst the row address is compared with the previously used row address, that is stored in an internal register. If the row addresses are identical, the $\overline{\text{RAS}}$ signal can remain low, thus saving the time for the row access.

ETRAX 100 supports both Fast page mode and Hyper page mode (EDO) DRAM chips. The timing diagram for a Fast page mode read cycle is shown in Figure 3-4.

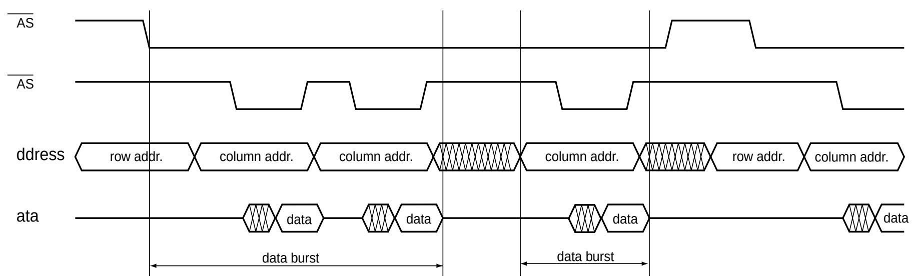

Figure 3-4 Timing diagram for Fast page mode read cycles

If EDO DRAM chips are used, ETRAX 100 uses the $\overline{\text{RAS}}$ signal or the $\overline{\text{DRAMWE}}$ signal to tell the DRAM to release the data bus. The DRAM will release the data bus either when the $\overline{\text{RAS}}$ signal goes high or when the $\overline{\text{DRAMWE}}$ signal goes low.

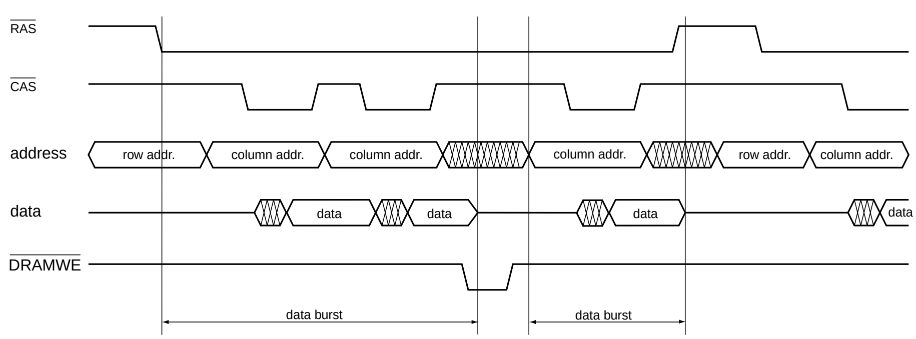

Figure 3-5 Timing diagram for EDO mode read cycles

3.7.1 Connecting the DRAM banks

The four DRAM banks are combined in two groups, with two banks in each group. Both banks in one group must have the same number of column address bits.

When accessing the DRAM banks, the $\overline{CAS}$ signals can be used either as bank strobes (bankwise $\overline{CAS}$ mode) or as byte strobes (bytewise $\overline{CAS}$ mode). One mode is used throughout a single application.

Bytewise $\overline{CAS}$ mode is illustrated in Figure 3-6. Only one $\overline{RAS}$ signal a time will be active in each group. The $\overline{CAS}$ signals are used to select the different bytes within the word or dword.

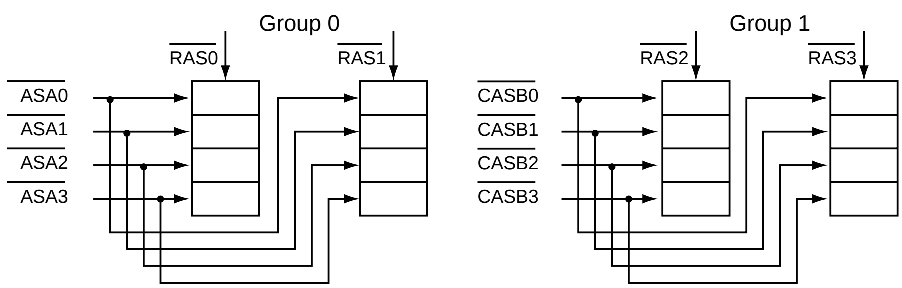

Figure 3-6 Bytewise $\overline{CAS}$ mode.

In a design using bankwise $\overline{CAS}$ mode, as in Figure 3-7, all the $\overline{RAS}$ signals can be active simultaneously. $\overline{CASA}$ decides which bank to access. If bytewise access is required, the byte $\overline{CAS}$ are generated by gating $\overline{CASB}$, used as byte enables, and $\overline{CASA}$ as shown in Figure 3-8.

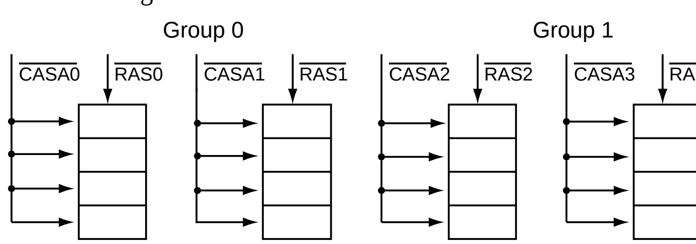

Figure 3-7 Bankwise accessing of DRAM modules.

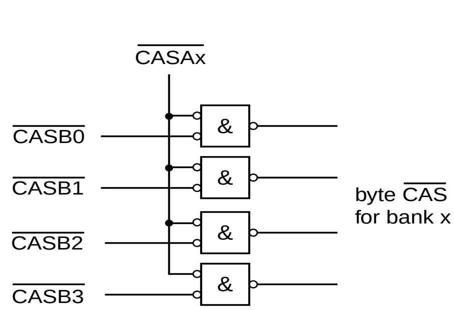

Figure 3-8 Generating byte $\overline{CAS}$.

When using 64-bit wide DRAM modules one $\overline{RAS}$ signal is assigned to each bank and this signal controls all 64 bits. Only one $\overline{RAS}$ is active at a time. The $\overline{CAS}$ signals are used to select the different bytes within the word, see Figure 3-9. The upper and lower 32 bits are tied together. That is, bit 0 and bit 32 are tied together and one at the time drives the databus. Bit 1 and bit 33 are tied together, etc.

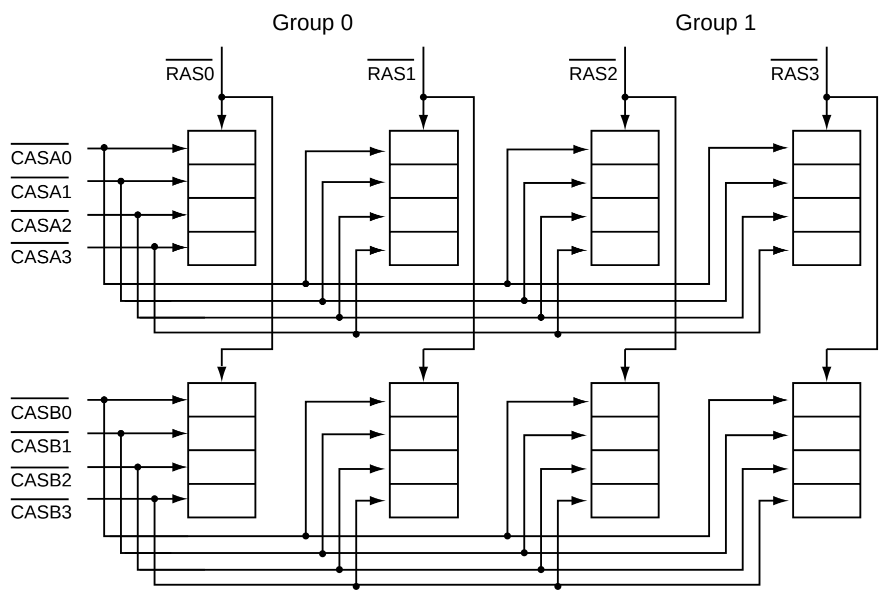

Figure 3-9 64-bit wide DRAM modules, all $\overline{CAS}$ signals used for selecting bytes.

In bankwise mode with 64-bit wide modules, the $\overline{CAS}$ signals are used to activate 32 bits at a time, as shown in Figure 3-10. In this case all $\overline{RAS}$ signals can be active at the same time, but it is not possible to select the separate bytes in the DRAM.

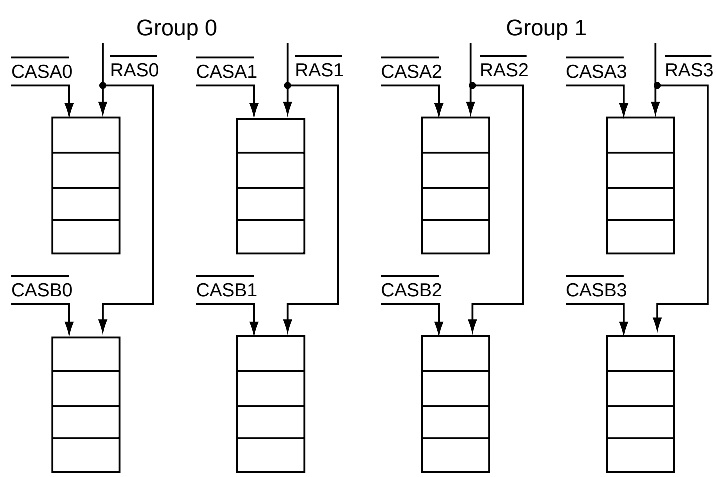

Figure 3-10 Bankwise accessing, 64-bit wide DRAM modules.

3.7.2 DRAM Bank Configuration

The four DRAM banks are combined in two groups with banks 0 and 1 in group 0 and banks 2 and 3 in group 1. The two banks in a group always share the same configuration.

Common to all banks, the following configurations are available:

Width (1 bit)

Selects 16- or 32-bit DRAM bus width.

0	16-bit DRAM bus width
1	32-bit DRAM bus width

EDO or Fast page mode (1 bit)

0	Fast page mode
1	EDO mode.

$\overline{\text{CAS}}$ organization (1 bit)

0	The $\overline{\text{CAS}}$ outputs are used for selecting bytes as in Figure 3-6 or, if wide module mode is selected, as in Figure 3-9.
1	One $\overline{\text{CAS}}$ output for each bank, see Figure 3-7 and Figure 3-8, or if wide module mode is selected, two $\overline{\text{CAS}}$ outputs per bank as in Figure 3-10.

Group select mode (5 bits)

The group select mode determines how to select group of DRAM banks:

Value	Select
0	Always select group 0
1	Always select group 1
2-8	Reserved
9-29	The internal address bit number corresponding to the select mode value is used to select group
30-31	Reserved

The following configurations are available for each group individually:

Row address shift (3 bits)

During the $\overline{RAS}$ portion of the cycle, the row portion of the internal address is shifted down to the lower address outputs to which the DRAM address pins are connected. The value given decides how many steps the address bits are shifted:

Value	Shift
0	Internal address bits 29 - 9 shifted down to pins A21 - A1.
:	:
:	:
7	Internal address bits 29 - 16 shifted down to pins A14 -A1, and pins A21 - A15 is set to 0 (zero).

(The internal address bits 25 - 22 are output on pins A25 - A22 during $\overline{RAS}$ cycles.)

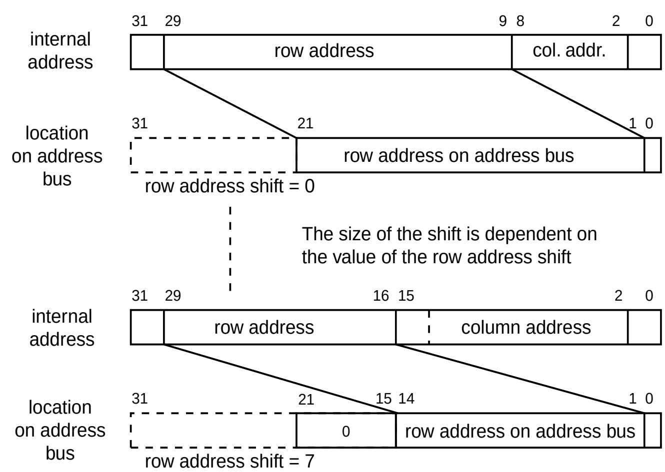

Figure 3-11 To accomplish the multiplexing of the row address and the column address on the address bus pins, the row address is shifted down to the lower pins of the bus during the $\overline{RAS}$ portion of the bus cycle.

Column address range (3 bits)

The column address range determines how many address bits that are used in the column address.
The ranges selected for the column address and the row address may overlap by one bit. When the row address has been shifted down, this bit corresponds to bit 1 on the address bus, that is not used in the 32-bit address. Consequently the overlapping bit is part of the column address.
There may also be a gap between the row address and column address parts, that are not used by the DRAM chip. The bits in the gap can be used to select bank and/or group.
In wide module mode, the selection between $\overline{CASA}$ and $\overline{CASB}$ is done by the highest address bit given by the column address range.The column address range should in this case be set to one higher than the actual highest column

address bit to the DRAM.

Value	Column address bits
0	Up to and including address bit 8
:	:
:	:
7	Up to and including address bit 15

Bank decode mode (5 bits)

The bank decode mode determines how to select between the two banks in a group:

Value	Select
0	Always select bank 0 (group 0) or bank 2 (group 1)
1	Always select bank 1 (group 0) or bank 3 (group 1)
2-8	Reserved
9-29	The internal address bit number corresponding to the decode mode value is used to select bank
30-31	Reserved

Wide module mode (1 bit)

This mode supports 64-bit wide DRAM modules, where all 64 bits are controlled by the same $\overline{\text{RAS}}$ signal. Both $\overline{\text{CASA}}$ and $\overline{\text{CASB}}$ are used within both groups of DRAM banks.
If bankwise $\overline{\text{CAS}}$ mode is combined with wide module mode in any of the two groups, none of the groups can use $\overline{\text{CASB}}$ as byte enables, see Figure 3-10 on page 35.

Value:	Select mode:
0	Normal mode
1	Wide module mode

3.8 EXTERNAL INTERRUPT ACKNOWLEDGE

If the external interrupt is configured for external vector number, an interrupt acknowledge cycle will occur when the interrupt is granted. During the interrupt acknowledge cycle, an 8-bit vector number is read on the low byte of the data bus. The cycle is indicated by the $\overline{\text{INTA}}$ signal going low. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are high during the cycle. The address and chip selects are undefined. Maximum timing is used for the INTA cycle, regardless of setting: ew = 3, lw = 15, zw = 3.

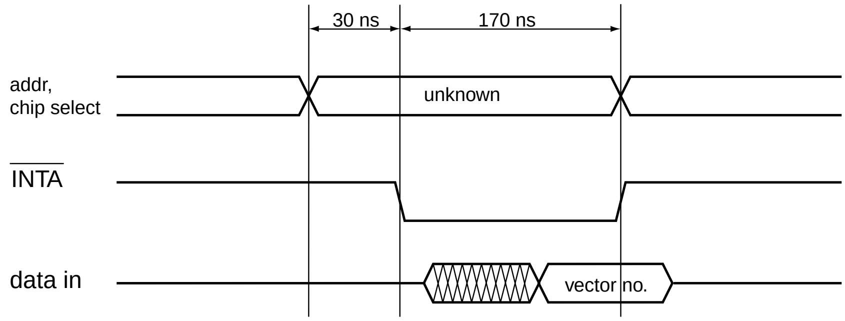

Figure 3-12 External $\overline{INTA}$ cycle

3.9 ACCESS TO INTERNAL I/O

Data read from or written to an internal I/O unit is present on the data bus for 2 clock cycles i.e. 20 ns. The $\overline{RD}$ pulse is active for 20 ns and the $\overline{WR}$ pulse is active for 20 ns. All chip selects are inactive.

3.10 WAIT INPUT AND BUS CYCLE RERUN

An external wait pin ($\overline{WAIT}$) is provided, that can be used by external devices to insert extra wait states. The $\overline{WAIT}$ input is fully synchronized. $\overline{WAIT}$ is sampled 3 clock cycles (30 ns) before the end of the bus cycle. Because of this, the use of the $\overline{WAIT}$ input requires that the number of internal wait states (ew + lw) for the memory area in question is set to 3 or more.

If the $\overline{WAIT}$ input is active for too long, it can cause overrun/underrun errors e.g. in the network interface. The maximum allowed active time is therefore limited, depending on the application.

For very slow external units it is possible to make a bus cycle rerun. It only applies for non-cacheable CPU accesses and is not allowed to be used on other types of cycles, like DMA cycles etc. The $\overline{RERUN}$ input is sampled at the rising edge of the $\overline{WAIT}$ signal. If it is sampled low the CPU will rerun the bus cycle.