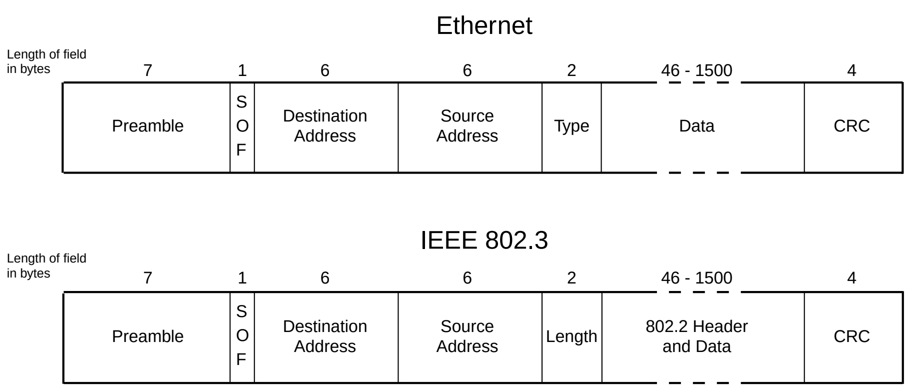
6 NETWORK INTERFACE

The ETRAX 100 includes an on-chip Fast Ethernet controller.

The ETRAX 100 network interface supports 10 and 100 Mbit/s Ethernet (IEEE 802.3 and Ethernet II) protocols. With 10 Mbit/s, the physical interface can be configured either to be compatible with 802.3 MII or SNI (National Semiconductor DP8391 compatible interface). 100 Mbit/s is only supported over 802.3 MII.

6.1 ETHERNET AND IEEE 802.3

There are some minor differences between the IEEE 802.3 standard and the Ethernet regarding the frames. Below is a figure that shows the frame format for the Ethernet and the frame format for the IEEE 802.3 standard.



SOF = Start-of-Frame Delimiter
CRC = Cycle Redunancy Check (same as FCS = Frame Check Sequence)

Figure 6-1 A description of the frames in Ethernet and the IEEE 802.3 standard

Table 6-1 give short explanations to the contents of the frames.

Frame fields	Description	Length (bytes)
Preamble Start-of-Frame Delimiter (SOF)	Provides synchronization. Consists of 7 (IEEE 802.3) or 8 (Ethernet) bytes of the bit pattern "10101010". Provides framing. Contains the bit pattern "10101011".	7 1
Destination Address	The address of the destination Network Interface Card (NIC) in the PC. The first bit indicates: 0 = individual; 1 = group address	6
Source Address	The address of the sending station.	6
Length or type	Specifies the length or type of the data field.	2
Data Pad	The data content. If the actual data is less than 46 bytes, pad bytes consisting of zeros are added up to the required minimum of 46 bytes.	46 - 1500 0 - 46
CRC, Frame Check	Used for error checking at the destination station. (CRC = Cyclic Redundancy Check)	4

Table 6-1 Explanations of the frame contents

6.2 RECEIVER LOGIC FUNCTIONS

The receiver logic of the network interface in ETRAX 100 performs the following:

- communicates the incoming data to the receiving FIFO.
- communicates status to the DMA channel controlling the receiving FIFO.
- checks the destination address of the incoming frame.
- checks the CRC of the incoming frame.
- checks the length of the incoming frame.

6.2.1 Data Transfer to the Receiving FIFO

When the receiver is enabled, the incoming data is transferred, one byte at a time, to the receiving FIFO. If the destination address of the frame does not match the address in the network interface, or if there is an error in the frame, the frame is aborted and the remaining bytes in the frame are not sent to the FIFO.

The frame sent to the FIFO contains the following:

DA	Destination address (6 bytes)
SA	Source address (6 bytes)
L	Length or type (2 bytes)
Data	Frame data (+ pad if necessary) (46 to 1500 bytes)
CRC	Cyclic redundancy check (4 bytes)

Table 6-1 The Frame sent to the FIFO

6.2.2 Address Recognition

The destination address (DA) field of the incoming frame is compared with the addresses set in the network interface. If the addresses do not match, the frame is aborted. Within the frame formats of the IEEE 802.3 standard, the destination address are of three types: individual address (unicast), group address (multicast) and broadcast (all nodes), as given in the table below.

Individual address	ETRAX 100 can hold two individual addresses, MA0 and MA1, each 48 bits long. All 48 bits are compared in each address. This means that one or both of the individual addresses can be used to match a group address instead. There is also one mode bit for each individual address to enable/disable recognition.
Group address	A 6-bit hash address is calculated from the 48 destination address (DA) bits: Hash_address<5:0> = DA<5:0> XOR DA<11:6> XOR DA<17:12> XOR DA<23:18> XOR DA<29:24> XOR DA<35:30> XOR DA<41:36> XOR DA<47:42> The hash address is used as an index into a 64-bit table, which indicates whether to copy the frame or not. There is also a mode bit to select whether to only match group addresses (DA<47> == 1) or to also match individual addresses.
Broadcast address	There is a mode bit to enable/disable the recognition of the broadcast address 0xFFFFFFFFFFFF.

Figure 6-1 The different destination addresses

6.2.3 Receiver CRC Check.

The incoming data is CRC checked according to the IEEE 802.3 standard. If an incorrect CRC is detected, the frame is aborted, and the CRC error counter or alignment error counter is updated.

With MII interface, the CRC block also monitors the RXER signal. If the RXER occurs during a reception, this is handled as if an incorrect CRC occurred.

There is a mode bit that enables/disables the abortion of frames due to incorrect CRC. If disabled, frames with CRC and alignment errors will also be received. Two status bits (the CRC error and the alignment error) are transferred to the

DMA channel. The DMA will put this status information in the status field of the DMA descriptor for the received frame.

6.2.4 Received Frame Length Check

The lengths of the incoming frames are checked against the specified limits of the IEEE 802.3 frame format.

Minimum: 64 bytes
Maximum: 1518 bytes

If the frame length is outside the specified bounds, the frame is aborted. There are two mode bits to enable the minimum length and maximum length check separately.

6.3 TRANSMITTER LOGIC FUNCTIONS

The transmitter logic block performs the following functions:

- Adds preamble and start of frame delimiter to the beginning of the frame.
- Calculates and adds CRC to the end of the frame.
- Pads frame data with zeros if the length of the frame data falls below the required minimum of 46 bytes.
- Handles the access protocol including automatic retransmission (CSMA/CD or demand priority).

6.3.1 Transmission of Frames

Transmit data is read from the FIFO, one byte at a time. The frame from the FIFO should contain the following:

DA	Destination address (6 bytes)
SA	Source address (6 bytes)
L	Length or type (2 bytes)
Data	Frame data (0 to 1500 bytes) (See note)

Table 6-2 The Frame from the FIFO

Note: Minimum length of data is 46 bytes if automatic pad is not selected.

The transmitter adds the preamble and start-of-frame delimiter to the beginning of the frame, and the frame check sequence (CRC) to the end of the frame. There is an option to automatically add a pad before the CRC if the data field of the frame is shorter than 46 bytes. The pad consists of all 0's.

With the MII interface it is possible to deliberately corrupt a frame by setting the TX_ERR bit (force network transmission error) in the DMA descriptor. The automatic addition of CRC to the frame can be disabled by a mode bit, and thus allowing to send corrupted frames, e.g. for test purposes.

If the transmitter gets a FIFO empty status during transmission without also getting an EOP, the transmission is stopped and the transmit underrun interrupt is activated. The transmitter remains stopped until the interrupt is cleared.

6.3.2 CSMA/CD Access Protocol

The CSMA/CD access protocol is used in IEEE 802.3 mode. The protocol listens continuously to carrier sense to see if the line is free. When a frame is queued for transmission, it is sent as soon as the line is free.

If a collision is detected during the transmission, the protocol tries to resend the frame 15 times, i.e. a total of 16 attempts are being made. If the transmission is aborted due to excessive collisions, the excessive retry interrupt is issued, and the transmitter stops. The transmitter remains stopped until the interrupt is cleared.

There are three mode bits that modify the access protocol handling. They can be used for other standard modes, as well as for test purposes or to implement protocols that deviate from the standard.

1. Full duplex mode can be used. In this mode, the carrier sense is ignored and there is no transmission deference. The collision signal is also ignored since collisions are not possible in full duplex mode. There is also a flow control mechanism in full duplex mode. This flow control is to avoid congestion of data transmitted from the ETRAX 100, and is achieved by using a PAUSE command which tells the transmitter to stop transmitting frames for a specified amount of time.
2. Retransmission can be disabled. The excessive retry interrupt will then be issued after the first collision.
3. A pending frame can be cancelled. This will inhibit any attempts to start sending a frame. If there is data in the FIFO but the transmission has not started, the frame will be aborted. If the transmission is already started it will be completed. No transmit retries will be made if the cancel bit is set. After the current frame is completed or aborted, the excessive retry interrupt will be issued.

6.3.3 Demand Priority Access Protocol

Demand priority access protocol is used in IEEE 802.12 mode. ETRAX 100 is designed to support this mode together with Texas Instruments TNETE211 (100-VG-AnyLAN2 PMD interface) or equivalents.

The Ethernet controller also supports the token ring frame format through an extended 802.3 MII interface, using a handshake protocol.

For more information about the operation in these modes please contact Axis Communications.

6.4 MANAGEMENT INTERFACE

The MII management interface consists of two pins, MDIO and MDCLK. These pins are controlled by software.

As an extension of the IEEE 802.3 management protocol, an interrupt is also implemented on the MDIO pin. An MDIO interrupt will be issued if the MDIO line is sampled low while the interrupt is enabled.

In SNI mode, the management interface in ETRAX 100 also includes the possibility to use MII_TXD<3:1> and TX_ERR as general outputs and to use MII_RXD<3:1> and RX_ERR as general inputs.

6.5 PIN USAGE IN MII AND SNI MODES

Pin name	Direction	MII usage	SNI usage
RXDATA0	in	Data in bit 0	Data in.
RXDATA3-1	in	Data in bit 3:1	General inputs
RXDV	in	Data in valid	Not used
RXER	in	Data in error	General input
RXCLK	in	Receive clock	Receive clock
TXDATA0	out	Data out bit 0	Data out
TXDATA3-1	out	Data out bit 3:1	General outputs
TXEN	out	Transmit enable	Transmit enable
TXER/ MIICLK/ AREC	out	Transmit error/ 25 MHz clock/ Address recognized	General output
TXCLK	in	Transmit clock	Transmit clock
CRS	in	Carrier sense	Carrier sense
COL	in	Collision	Collision
MDCLK	out	Management clock	General output
MDIO	in/out	Selects SNI or MII during bootstrap/Management data	Selects SNI or MII during bootstrap/General I/O

Table 6-3 Pin Usage in MII and SNI Modes

6.6 INTERNAL LOOPBACK MODE

The network interface can also be set in an internal loopback mode, where the transmit data is fed directly to the receiver. The data speed in internal loopback mode is 100 Mbit/s.

6.7 ETHERNET ERROR AND STATISTICS COUNTERS

ETRAX 100 contains the following Ethernet error and statistics counters:

Counter	Explanation
crc_error	Number of frames with crc errors
alignment_error	Number of frames with alignment errors
oversize	Number of oversized frames
congestion	Number of otherwise correct frames that were not received due to a FIFO full condition
single_col	Number of frames that were involved in exactly one collision
multiple_col	Number of frames that were involved in more than one collision
late_col	Number of frames that were involved in late collisions
deferred	Number of deferred transmit frames
carrier_loss	Number of transmit frames for which the carrier sense signal was not constantly present during the transmission
sqe_test_error	Number of transmitted frames for which the sqe test signal was not recognized

Table 6-4 Ethernet error and statistics counters

Each counter is 8 bits wide. The counters are cleared either when read or at system reset. When a counter reaches 255 it stops counting. If the network interface is disabled the counter values are preserved.

An interrupt is generated for a counter when it reaches 128. Reading the counter will clear the associated interrupt. The interrupt status can be masked individually, but all counters share a common interrupt vector number.

The congestion error counter also generates an interrupt whenever the count is anything else than zero. This interrupt can be masked separately, and shares interrupt vector number with the excessive retry, transmit underrun and MII management interrupts.

6.8 NETWORK INTERRUPTS

6.8.1 Overrun

The overrun interrupt is set when the receiver cannot handle the data as fast as it is coming in. A congestion error is the same as an overrun interrupt.

6.8.2 Underrun

The underrun interrupt is set when the transmitter cannot transmit data at the network bandwidth. The conditions for an underrun interrupt is when the transmitter gets a FIFO empty status during transmission without also getting an EOP. If this happens the transmission is stopped and the transmit underrun interrupt is activated. The transmitter remains stopped until the interrupt is cleared.

6.8.3 Excessive collision

An excessive collision interrupt occurs when a packet could not be transmitted after 16 attempts due to repeated collisions.

6.8.4 MDIO

The MDIO is an interrupt signal used with the MII interface.