

# 11 SHARED RAM INTERFACE

The shared RAM interface handles 8-bit and 16-bit transfers between an external device and the system SRAM. The interface operates with standard SRAM. Data transfers are controlled by an asynchronous handshake protocol.

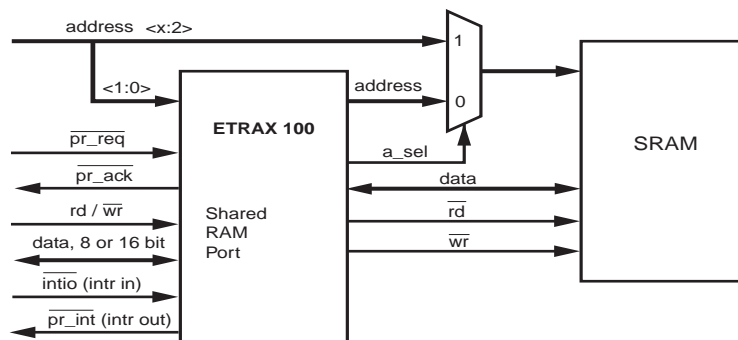


Figure 11-1 How to connect for shared RAM

The address from the external device is supplied to the SRAM through external multiplexers, except for address bit 0 and 1 that are multiplexed internally.

Shared RAM interface cycles are like normal bus cycles, except that the  $\overline{A\_SEL}$  signal on the  $\overline{s0atn}$  pin is high during the cycle. Shared RAM interface cycles are never packed together in bursts. The cycles can be 8-bit or 16-bit wide. 16-bit cycles are always 16-bit aligned.

One interrupt signal in each direction is provided. The interrupt going out is active low and stays low for 600 ns. The incoming interrupt is negative edge triggered.

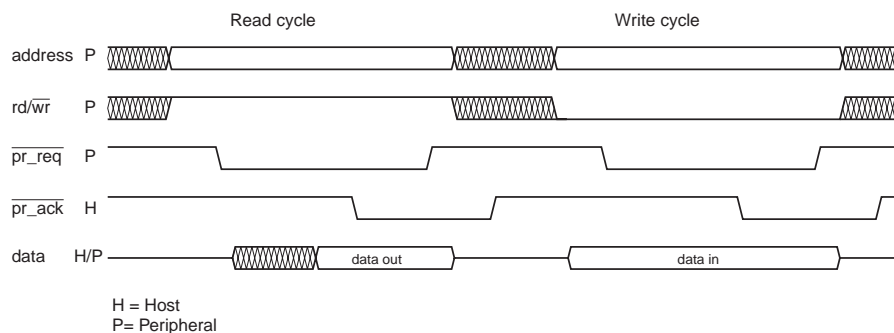


Figure 11-2 Shared RAM timing

