12 TIMERS

12.1 GENERAL

The timer block consists of a clock divider, two programmable timers and one watchdog timer. The clock divider is also used as a baud rate generator for the serial ports. The two programmable timers can be cascaded to form one 16-bit timer.

12.2 CLOCK DIVIDER

The clock divider divides the internal clock down to the different frequencies required for the timers and serial ports.

At first, a 6.25 and a 14.75 MHz clock are generated. The 14.75 MHz clock is then further divided by two 8-bit binary up counters, fast and slow. The fast counter also has a divide-by-192 output, which is used as the input clock for the slow counter. The current value of the counters can be read in an internal register. The clock divider starts from 0 after reset.

The actual frequency is 64 ppm higher than the nominal value (given an exact clock reference input), for all frequencies except 6250 kHz. This deviation is in most cases negligible.

12.3 PROGRAMMABLE TIMERS

12.3.1 Timer Operation

ETRAX 100 has two programmable timers. Each one is an 8-bit binary down counter.

Each timer can be loaded with a divide factor between 1 and 256 (256 is achieved by loading 0 to the register). When started, the timer counts down to 1, and then generates an interrupt and restarts from the programmed divide factor. If the divide factor is changed while the timer is running, it will not take effect until the ongoing count has expired.

Each timer has two mode bits that control the operation:

Timer mode:	Operation:
00	Stop the timer and load it with the divide factor
01	Stop the timer and preserve current count value
10	Run
11	Reserved, do not use

Table 12-1 The timer modes

Each timer also has a “clear interrupt” mode bit. Setting it to 1 clears the interrupt, setting it to 0 has no effect.

The current count value of both timers can be read in an internal register.

12.3.2 Timer Input Clock

Input clock can be individually selected for each timer. The following input frequencies can be selected:

Clock sel:	Nominal frequency (see note):
0	0.3 kHz
1	0.6 kHz
2	1.2 kHz
3	2.4 kHz
4	4.8 kHz
5	9.6 kHz
6	19.2 kHz
7	38.4 kHz
8	57.6 kHz
9	115.2 kHz
10	230.4 kHz
11	460.8 kHz
12	921.6 kHz
13	1843.2 kHz
14	6250.0 kHz

Table 12-2 Available input frequencies

Note: The actual frequency is 64 ppm higher than the nominal value (given an exact clock reference input), for all frequencies except 6250 kHz.

12.3.3 Cascade Mode

The two programmable counters can be cascaded to form one 16-bit timer. Cascade mode is selected by setting the clock_sel bits for timer_1 to 15. The timer_0 interrupt is used to signal the end count of the cascaded counter. The timer_1 interrupt is not used in cascade mode.

When the counters operate in cascade mode, the timer modes should be set to the same value for both counters by one single write operation.

12.4 WATCHDOG TIMER

When the watchdog timer is started, it generates an NMI if the watchdog is not restarted or stopped within 0.1 s. If it still is not restarted or stopped after an additional 3.3 ms, the watchdog resets the chip. The watchdog timer is stopped after reset. The watchdog timer is controlled by an internal register, which contains an enable bit and a 3-bit key value. The effect of writing to the register is described in the table below:

Watchdog state:	Value written: To enable:	To key:	Operation:
stopped	0	X	No effect
stopped	1	key_val	Start watchdog with key = key_val
started	0	~key	Stop watchdog
started	1	~key	Restart watchdog with key = ~key
started	X	new_key_val	Change key to new_key_val

Table 12-3

Note : '~' is the bitwise NOT operator.