

13 GENERAL I/O

13.1 GENERAL

There are two 8-bit general I/O ports, PA and PB. They are always available and software controlled by setting registers. All other pins of the internal I/O units can also be used as general ports, if these pins are not used for any other purpose.

13.2 PORT PA

The 8 bits of port PA are individually configurable. The direction and the level of each bit is set in an internal register. The ports can be read in another register.

Each and every bit of the PA port can also be configured for incoming interrupts, to be level triggered on active high.

Each pin can supply a current of 12 mA which makes this port suitable for e.g. driving light emitting diodes.

13.3 PORT PB

The 8 bits of port PB can also be individually configured and the port can be read in a register. Directions and levels can be set, just as for port PA. Additionally, bits 2-7 can be used as chip selects (CSP 1-3, CSP 5-7). When software selectable ID is used for arbitration in SCSI, bits 4 and 7 control external buffers.

Bit 0 and 1 can be configured for the I2C interface. This makes it possible to run the I2C interface without having to check for interference with other bits in port PB. The bits of port PB can not be used for interrupts.

13.4 OTHER GENERAL PORTS

All pins that are not needed in the chosen configuration of the internal I/O units (SCSI, parallel ports etc.), can be used as general ports, see chapter Electrical Information, Multiplexed I/O Interfaces on page 115.

