

16 ELECTRICAL INFORMATION

16.1 PINOUT

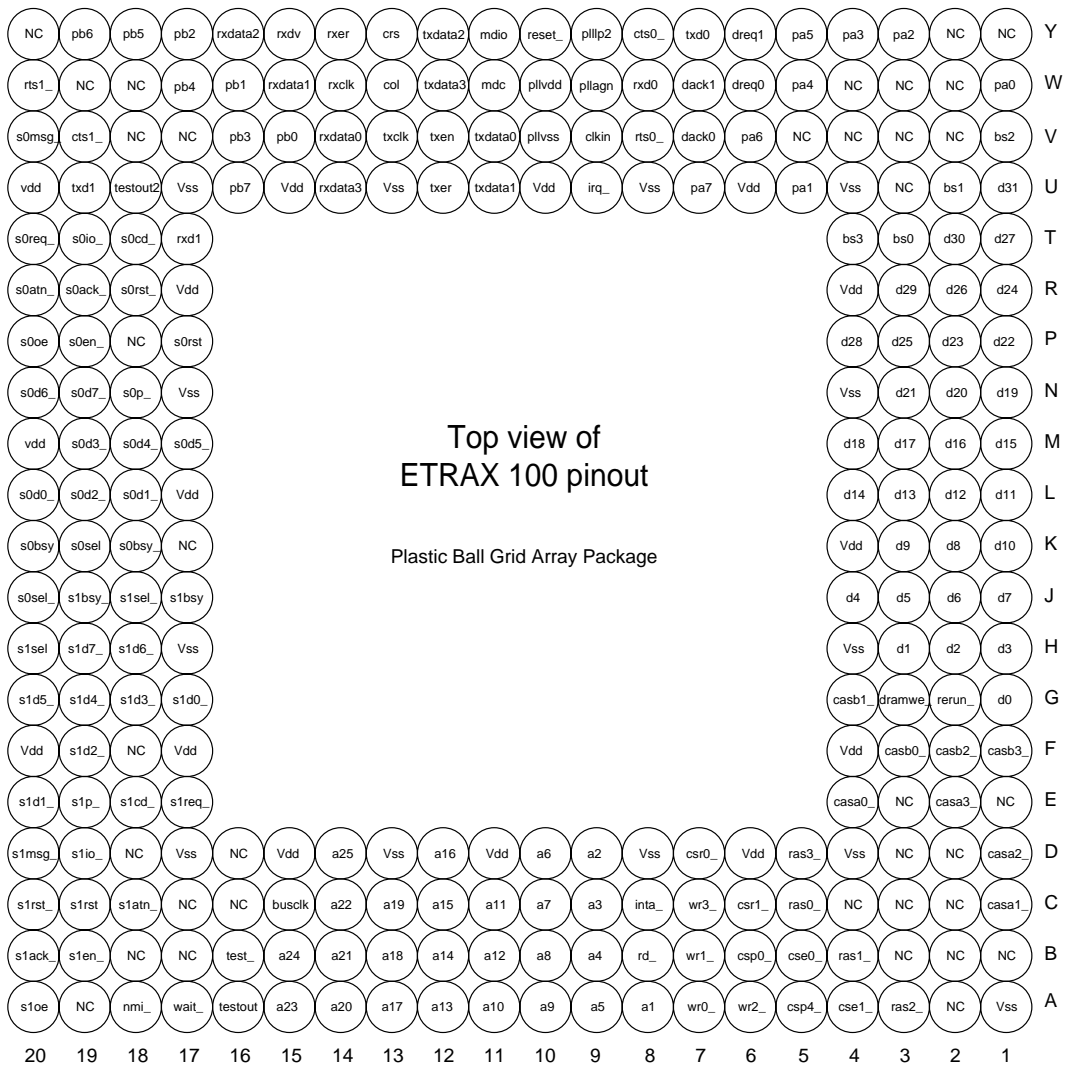


Figure 16-1 ETRAX 100 pinout

16.1.1 Clock and PLL

Solder Ball	Direction	Name	Description
V9	in	clkin	External clock input
W9	out	pllagn	PLL loop filter ground connection
Y9	inout	pllp2	PLL loop filter
W10	in	pllvdd	PLL supply voltage
V10	in	pllvss	PLL ground connection

Table 16-1 Clock and PLL

16.1.2 Power and Ground

Solder Ball	Name	Description
A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17	V _{ss}	Ground connection
D6, D11, D15, F4, F17, F20, K4, L17, M20, R4, R17, U6, U10, U15, U20	V _{dd}	Supply voltage, 3.3 V

Table 16-2 Power and Ground

16.1.3 Bus Interface Signals

Address Bus

Solder Ball	Direction	Name
D14	out	a25
B15	out	a24
A15	out	a23
C14	out	a22
B14	out	a21
A14	out	a20
C13	out	a19
B13	out	a18
A13	out	a17
D12	out	a16
C12	out	a15
B12	out	a14
A12	out	a13
B11	out	a12
C11	out	a11
A11	out	a10
A10	out	a9
B10	out	a8
C10	out	a7
D10	out	a6
A9	out	a5
B9	out	a4
C9	out	a3
D9	out	a2
A8	out	a1

Table 16-3 Address Bus

Data Bus

Solder Ball	Direction	Name
G1	inout	d0
H3	inout	d1
H2	inout	d2
H1	inout	d3
J4	inout	d4
J3	inout	d5
J2	inout	d6
J1	inout	d7
K2	inout	d8
K3	inout	d9
K1	inout	d10
L1	inout	d11
L2	inout	d12
L3	inout	d13
L4	inout	d14
M1	inout	d15
M2	inout	d16
M3	inout	d17
M4	inout	d18
N1	inout	d19
N2	inout	d20
N3	inout	d21
P1	inout	d22
P2	inout	d23
R1	inout	d24
P3	inout	d25
R2	inout	d26
T1	inout	d27
P4	inout	d28
R3	inout	d29
T2	inout	d30
U1	inout	d31

Table 16-4 Data Bus

Chip Select

Solder Ball	Direction	Name	Description
B6	out	$\overline{\text{csp0}}_-$	Peripheral select 0
A5	out	$\overline{\text{csp4}}_-$	Peripheral select 4
D7	out	$\overline{\text{csr0}}_-$	SRAM select 0
C6	out	$\overline{\text{csr1}}_-$	SRAM select 1
B5	out	$\overline{\text{cse0}}_-$	EPROM/flashPROM select 0
A4	out	$\overline{\text{cse1}}_-$	EPROM/flashPROM select 1

Table 16-5 Chip Select

Peripheral selects 1-3 and 5-7 are multiplexed with bits 2-7 in general port PB in the I/O block.

Read/Write Strobes

Solder Ball	Direction	Name	Description
B8	out	$\overline{\text{rd}}_-$	Read strobe, common to all four bytes of the data bus. Not active during DRAM access.
A7	out	$\overline{\text{wr0}}_-$	Write strobe for byte 0 of the data bus
B7	out	$\overline{\text{wr1}}_-$	Write strobe for byte 1 of the data bus
A6	out	$\overline{\text{wr2}}_-$	Write strobe for byte 2 of the data bus
C7	out	$\overline{\text{wr3}}_-$	Write strobe for byte 3 of the data bus

Table 16-6 Read/Write Strobes

DRAM Signals

Solder Ball	Direction	Name	Description
E4	out	$\overline{\text{casa0}}_-$	DRAM column address strobe, see note 1
C1	out	$\overline{\text{casa1}}_-$	DRAM column address strobe, see note 1
D1	out	$\overline{\text{casa2}}_-$	DRAM column address strobe, see note 1
E2	out	$\overline{\text{casa3}}_-$	DRAM column address strobe, see note 1
F3	out	$\overline{\text{casb0}}_-$	DRAM column address strobe, see note 2
G4	out	$\overline{\text{casb1}}_-$	DRAM column address strobe, see note 2
F2	out	$\overline{\text{casb2}}_-$	DRAM column address strobe, see note 2
F1	out	$\overline{\text{casb3}}_-$	DRAM column address strobe, see note 2
G3	out	$\overline{\text{dramwe}}_-$	DRAM write enable.
C5	out	$\overline{\text{ras0}}_-$	DRAM row address strobe for DRAM bank 0
B4	out	$\overline{\text{ras1}}_-$	DRAM row address strobe for DRAM bank 1
A3	out	$\overline{\text{ras2}}_-$	DRAM row address strobe for DRAM bank 2
D5	out	$\overline{\text{ras3}}_-$	DRAM row address strobe for DRAM bank 3

Table 16-7 DRAM Signals

Note 1: In byte-wise $\overline{\text{CAS}}$ mode $\overline{\text{casa0}}$ - $\overline{\text{casa3}}$ are the byte-wise $\overline{\text{CAS}}$ strobes for DRAM bank 0 and 1. In bank-wise $\overline{\text{CAS}}$ modes, they are the bank-wise $\overline{\text{CAS}}$ strobes for DRAM bank 0 to 3.

Note 2: $\overline{\text{casb0}}$ - $\overline{\text{casb3}}$ are the byte-wise $\overline{\text{CAS}}$ strobes for DRAM bank 2 and 3. In bank-wise $\overline{\text{CAS}}$ mode, the pins are redefined as $\overline{\text{be0}}$ - $\overline{\text{be3}}$, byte enables, one for each byte in the data bus.

Miscellaneous Bus Interface Signals

Solder Ball	Direction	Name	Description
G2	in	$\overline{\text{rerun}}_$	Bus rerun signal. If $\overline{\text{rerun}}$ is set low together with $\overline{\text{wait}}$, the current bus cycle is terminated without completion, and will be restarted later. This only works for non-cacheable CPU accesses, not for DMA cycles or cache bursts.
W6	in	dreq0	DMA request, external DMA0
Y6	in	dreq1	DMA request, external DMA1
V7	out	dack0	DMA acknowledge, external DMA0
W7	out	dack1	DMA acknowledge, external DMA1
U9	in	$\overline{\text{irq}}_$	Interrupt request
A18	in	$\overline{\text{nmi}}_$	Non maskable interrupt request
A17	in	$\overline{\text{wait}}_$	External wait state input
C8	out	$\overline{\text{inta}}_$	External interrupt acknowledge
Y10	in	$\overline{\text{reset}}_$	System reset

Table 16-8 Miscellaneous Bus Interface Signals

16.1.4 Logic Analyzer Mode and Test

Solder Ball	Direction	Name	Description
T3	inout	bs0	Bus status, bit 0, see note
U2	inout	bs1	Bus status, bit 1, see note
V1	inout	bs2	Bus status, bit 2, see note
T4	inout	bs3	Bus status, bit 3, see note
B16	in	$\overline{\text{test}}_$	Test input, should be high for normal operation
A16	out	testout	Test output, must not be connected
C15	out	busclk	Bus synchronization clock. Used for debug purposes.
U18	out	testout2	Test output, must not be connected

Table 16-9 Logic Analyzer Mode and Test

Note: Input for bus configuration during power on reset. Used as status outputs for debug purposes when reset is inactive.

16.1.5 General Ports PA and PB

Solder Ball	Direction	Name	Description
W1	inout	pa0	General port PA, bit 0
U5	inout	pa1	General port PA, bit 1
Y3	inout	pa2	General port PA, bit 2
Y4	inout	pa3	General port PA, bit 3
W5	inout	pa4	General port PA, bit 4
Y5	inout	pa5	General port PA, bit 5
V6	inout	pa6	General port PA, bit 6
U7	inout	pa7	General port PA, bit 7
V15	inout	pb0	General Port PB, bit 0/I2C data
W16	inout	pb1	General Port PB, bit 1/I2C clock
Y17	inout	pb2	General Port PB, bit 2/Peripheral select 1
V16	inout	pb3	General Port PB, bit 3/Peripheral select 2
W17	inout	pb4	General Port PB, bit 4/Peripheral select 3/SCSI0 phase enable for software ID select
Y18	inout	pb5	General Port PB, bit 5/Peripheral select 5
Y19	inout	pb6	General Port PB, bit 6/Peripheral select 6
U16	inout	pb7	General Port PB, bit 7/Peripheral select 7/SCSI1 phase enable for software ID select

Table 16-10 General ports PA and PB

16.1.6 Serial Ports 0 and 1

Solder Ball	Direction	Name	Description
Y7	out	txd0	Transmit data, serial port 0
V8	out	rts0_	Request to send, serial port 0
W8	in	rxd0	Receive data, serial port 0
Y8	in	cts0_	Clear to send, serial port 0
U19	out	txd1	Transmit data, serial port 1
W20	out	rts1_	Request to send, serial port 1
T17	in	rxd1	Receive data, serial port 1
V19	in	cts1_	Clear to send, serial port 1

Table 16-11 Serial ports 0 and 1

Note 1: Serial ports 2 and 3 are multiplexed on pins used by a number of other I/O-interfaces, see Multiplexed I/O Interfaces on page 111.

Note 2: The default values of serial ports 0 and 1 is undefined. The default values of the multiplexed serial ports 2 and 3 is described in "Serial Ports 2 and 3" on page 121.

16.1.7 Network interface

Solder Ball	Direction	Name	MII usage	SNI usage
Y11	inout	mdio	Management data	General I/O
W11	out	mdc	Management clock	General output
V11	out	txdata0	Data out, bit 0	Data out
U11	out	txdata1	Data out, bit 1	General output
Y12	out	txdata2	Data out, bit 2	General output
W12	out	txdata3	Data out, bit 3	General output
V12	out	txen	Transmit enable	Transmit enable
U12	out	txer	Transmit error/ 25 MHz clock/ Address recognized	General output
Y13	in	crs	Carrier sense	Carrier sense
W13	in	col	Collision	Collision
V13	in	txclk	Transmit clock	Transmit clock
Y14	in	rxer	Receive error	General input
W14	in	rxclk	Receive clock	Receive clock
Y15	in	rxdv	Data in valid	Not used
V14	in	rxdata0	Data in, bit 0	Data in
W15	in	rxdata1	Data in, bit 1	General input
Y16	in	rxdata2	Data in, bit 2	General input
U14	in	rxdata3	Data in, bit 3	General input

Table 16-12 Network interface

16.1.8 Multiplexed I/O Interfaces

The I/O applications given in the table 16-13 are multiplexed on the I/O pins.

Application	Description
Serial p2 Serial p3	Serial ports.
Shared RAM Shared RAM-W	8 bit Shared RAM interface 8 bit Shared RAM extended to 16 bit. (Only useful together with Shared RAM.)
Parallel p0 Parallel p1	Parallel printer ports.
SCSI-8 p0 SCSI-8 p1	8 bit SCSI ports.
SCSI-W	16 bit SCSI.
ATA	ATA interface.
General I/O	General I/O pins.

Table 16-13 Multiplexed I/O Interfaces

A subdivision of all multiplexed I/O pins has been done into four groups: Group A (19 pins); Group B (4 pins); Group C (4 pins); and Group D (19 pins). This subdivision has been done according to the least number of pins used by any of these interfaces.

Group	A	B	C	D
No of pins	19 pins	4 pins	4 pins	19 pins
Serial ports		Ser. p2	Ser. p3	
Shared RAM	Shared RAM			
Shared RAM-W	Shared RAM-W			Shared RAM-W
Parallel ports	Parallel port p0			Parallel port p1
SCSI-8	SCSI-8 p0			SCSI-8 p1
SCSI-W		SCSI-W		
ATA		ATA		
General I/O		General I/O		

Table 16-14 The four groups of the multiplexed I/O interfaces

Table 16-14 shows, for instance, that it is not possible to use SCSI-8 p0 and on the same time serial port 2, since the four pins used by the serial port 2 are also used by the SCSI-8 p0 interface.

Pins not used in a specific interface e.g. ATA or the parallel ports, are available for General I/O (e.g. g25 - g28 are available in ATA mode). However, in regard to the ATA interface no other interfaces or pins can be used than those listed in the column for the ATA interface in table 16-15 on page 113. For instance, if the ATA interface is connected to handle only one disk drive, and group A, B and D are used, the General I/O in group C is not available.

Please use the table 16-15 on page 113 for reference.

Group A

Solder Ball	SCSI-8 p0		SCSI-W		ATA		Par. p0		Shared RAM		Gen. I/O	
V20	s0msg_	inout	s0msg_	inout	ioridy	in	p0perror_	in	pr_adr0	in	g5	in
T18	s0cd_	inout	s0cd_	inout	dmarq0	in	p0ack_	in	pr_adr1	in	g4	in
T19	s0io_	inout	s0io_	inout	dmarq1	in	p0busy	in	intio_	in	g3	in
T20	s0req_	in	s0req_	in	dmarq2	in	p0fault_	in	rd_wr	in	g2	in
R18	s0rst_	in	s0rst_	in	dmarq3	in	p0select	in	pr_req_	in	g1	in
P17	s0rst	out	s0rst	out	cs0_	out	p0data_oe	out	pr_int_	out	g5	out
R19	s0ack_	out	s0ack_	out	cs1_	out	p0selectin_	out	pr_ack_	out	g4	out
R20	s0atn_	out	s0atn_	out	a0	out	p0autofd_	out	a_sel	out	g3	out
K20	s0bsy	out	s0bsy	out	a1	out	p0strobe_	out	g2	out	g2	out
P20	s0oe	out	s0oe	out	a2	out	p0init_	out	g1	out	g1	out
N18	s0p_	inout	s0p_	inout	dmack0_	out	g0	inout	g0	inout	g0	inout
N19	s0d7_	inout	s0d7_	inout	d7	inout	p0d7	inout	pr_d7	inout	g15	inout
N20	s0d6_	inout	s0d6_	inout	d6	inout	p0d6	inout	pr_d6	inout	g14	inout
M17	s0d5_	inout	s0d5_	inout	d5	inout	p0d5	inout	pr_d5	inout	g13	inout
M18	s0d4_	inout	s0d4_	inout	d4	inout	p0d4	inout	pr_d4	inout	g12	inout
M19	s0d3_	inout	s0d3_	inout	d3	inout	p0d3	inout	pr_d3	inout	g11	inout
L19	s0d2_	inout	s0d2_	inout	d2	inout	p0d2	inout	pr_d2	inout	g10	inout
L18	s0d1_	inout	s0d1_	inout	d1	inout	p0d1	inout	pr_d1	inout	g9	inout
L20	s0d0_	inout	s0d0_	inout	d0	inout	p0d0	inout	pr_d0	inout	g8	inout

Group B

Solder Ball	SCSI-8 p0		SCSI-W		ATA		SER p2		Gen. I/O		
P19	s0en_	out	s0en_	out	dior0_	out	rts2_	out		g7	out
K19	s0sel	out	s0sel	out	dior1_	out	txd2	out		g6	out
K18	s0bsy_	in	s0bsy_	in	intrq0	in	cts2_	in		g7	in
J20	s0sel_	in	s0sel_	in	intrq1	in	rxd2	in		g6	in

Group C

Solder Ball	SCSI-8 p1		SCSI-W		ATA		SER p3		Gen. I/O		
J19	s1bsy_	in	g31	in	intrq2	in	cts3_	in		g31	in
J18	s1sel_	in	g30	in	intrq3	in	rxd3	in		g30	in
B19	s1en	out	g31	out	dior2_	out	rts3_	out		g31	out
H20	s1sel	out	g30	out	dior3_	out	txd3	out		g30	out

Group D

Solder Ball	SCSI-8 p1		SCSI-W		ATA		PAR p1		Shared RAM-W		Gen. I/O	
H19	s1d7_	inout	s0d15_	inout	d15	inout	p1d7	inout	pr_d15	inout	g23	inout
H18	s1d6_	inout	s0d14_	inout	d14	inout	p1d6	inout	pr_d14	inout	g22	inout
G20	s1d5_	inout	s0d13_	inout	d13	inout	p1d5	inout	pr_d13	inout	g21	inout
G19	s1d4_	inout	s0d12_	inout	d12	inout	p1d4	inout	pr_d12	inout	g20	inout
G18	s1d3_	inout	s0d11_	inout	d11	inout	p1d3	inout	pr_d11	inout	g19	inout
F19	s1d2_	inout	s0d10_	inout	d10	inout	p1d2	inout	pr_d10	inout	g18	inout
E20	s1d1_	inout	s0d9_	inout	d9	inout	p1d1	inout	pr_d9	inout	g17	inout
G17	s1d0_	inout	s0d8_	inout	d8	inout	p1d0	inout	pr_d8	inout	g16	inout
E19	s1p_	inout	s0p1_	inout	dmack1_	out	g24	inout	g24	inout	g24	inout
D20	s1msg_	inout	g29	in	dmack2_	out	p1perror_	in	g29	in	g29	in
E18	s1cd_	inout	g28	in	dmack3_	out	p1ack_	in	g28	in	g28	in
D19	s1io_	inout	g27	in	g27	out	p1busy	in	g27	in	g27	in
E17	s1req_	in	g26	in	g26	in	p1fault_	in	g26	in	g26	in
C20	s1rst_	in	g25	in	g25	in	p1select	in	g25	in	g25	in
C19	s1rst	out	g29	out	diow0_	out	p1data_oe	out	g29	out	g29	out
B20	s1ack_	out	g28	out	diow1_	out	p1selectin_	out	g28	out	g28	out
C18	s1atn_	out	g27	out	diow2_	out	p1autofd_	out	g27	out	g27	out
J17	s1bsy	out	g26	out	diow3_	out	p1strobe_	out	g26	out	g26	out
A20	s1oe	out	s1oe	out	ext_oe	out	p1init_	out	g25	out	g25	out

Table 16-15 The multiplexed interfaces

Default values of the multiplexed I/O pins

All bidirectional ports are by default inputs.

The output pins have the following default values:

Solder Ball	Default value	SCSI-8 p0 SCSI-W	SCSI-8 p1	Serial p2	Serial p3	ATA	Parallel p0	Parallel p1	Shared RAM	Gen I/O
P17	0	s0rst				cs0_	p0data_oe		pr_int_	g5
R19	0	s0ack_				cs1_	p0selectin_		pr_ack_	g4
R20	0	s0atn_				a0	p0autofd_		a_sel	g3
K20	0	s0bsy				a1	p0strobe_			g2
P20	0	s0oe				a2	p0init_			g1
P19	1	s0en_		rts2_		dior0_				g7
K19	0	s0sel		txd2		dior1_				g6
B19	1		s1en_		rts3_	dior2_				g31
H20	0		s1sel		txd3	dior3_				g30
C19	0		s1rst			diow0_		p1data_oe		g29
B20	0		s1ack_			diow1_		p1selectin_		g28
C18	0		s1atn_			diow2_		p1autofd_		g27
J17	0		s1bsy			diow3_		p1strobe_		g26
A20	0		s1oe			ext_oe		p1init_		g25

Table 16-16 Default values of the multiplexed output pins

16.1.9 I/O Application Multiplexed Signals

The IO applications in this section have their signals multiplexed as shown in table 16-15 on page 113.

8-bit SCSI Interface

SCSI 8-bit interface 0 consists of the following signals:

Solder Ball	Name	Direction	Description
V20	$\overline{s0msg_}$	in (out), see note 1	Message, driven by target during message phase
T18	$\overline{s0cd_}$	in (out), see note 1	Control/Data, driven by target to determine if control or data information is on the bus
T19	$\overline{s0io_}$	in (out), see note 1	Input/Output, driven by target and indicates bus direction.
R19	$\overline{s0ack_}$	out	Acknowledge signal in the information transfer handshake
T20	$\overline{s0req_}$	in	Request signal in the information transfer handshake
R20	$\overline{s0atn_}$	out	Attention condition indicator from host to target
K19	$\overline{s0sel}$	out	Select or reselect signal from SCSI interface to SCSI buffer.
J20	$\overline{s0sel_}$	in, see note 2	-SEL signal from SCSI bus to SCSI interface.
K20	$\overline{s0bsy}$	out	Bus in use signal from SCSI interface to SCSI buffer.
K18	$\overline{s0bsy_}$	in, see note 2	-BSY signal from SCSI bus to SCSI interface.
P17	$\overline{s0rst}$	out	Bus reset signal from SCSI interface to SCSI buffer.
R18	$\overline{s0rst_}$	in, see note 2	-RST signal from SCSI bus to SCSI interface.
N18	$\overline{s0p_}$	inout	Data bus parity
N19	$\overline{s0d7_}$	inout	Data bus
N20	$\overline{s0d6_}$	inout	
M17	$\overline{s0d5_}$	inout	
M18	$\overline{s0d4_}$	inout	
M19	$\overline{s0d3_}$	inout	
L19	$\overline{s0d2_}$	inout	
L18	$\overline{s0d1_}$	inout	
L20	$\overline{s0d0_}$	inout	
P20	$\overline{s0oe}$	out	External bus driver direction for $\overline{s0d0_}$ - $\overline{s0d7_}$, $\overline{s0p_}$ signals
P19	$\overline{s0en_}$	out	External driver output enable for $\overline{s0ack_}$, $\overline{s0atn_}$ signals

Table 16-17 SCSI port 0

Bit 4 on the General Port PB, is used as software ID output enable with SCSI interface 0 ($\overline{s0enph_}$). See pb4 in table 16-10 on page 110.

Note 1: If software ID is enabled, the host SCSI ID number is driven to the external logic during arbitration. See documentation about software ID and external buffer solution in Chapter 7, External SCSI Buffers on page 64.

Note 2: The SCSI bus OR-tied signals -SEL, -RST, and -BSY are being generated by the external SCSI buffer, see chapter 7.

SCSI 8-bit interface 1 consists of the following signals:

Solder Ball	Name	Direction	Description
D20	$\overline{s1msg_}$	in (out), see note 1	Message, driven by target during message phase
E18	$\overline{s1cd_}$	in (out), see note 1	Control/Data, driven by target to determine if control or data information is on the bus
D19	$\overline{s1io_}$	in (out), see note 1	Input/Output, driven by target and indicates bus direction.
B20	$\overline{s1ack_}$	out	Acknowledge signal in the information transfer handshake
E17	$\overline{s1req_}$	in	Request signal in the information transfer handshake
C18	$\overline{s1atn_}$	out	Attention condition indicator from host to target
H20	s1sel	out	Select or reselect signal from SCSI interface to SCSI buffer.
J18	$\overline{s1sel_}$	in, see note 2	-SEL signal from SCSI bus to SCSI interface.
J17	s1bsy	out	Bus in use signal from SCSI interface to SCSI buffer.
J19	$\overline{s1bsy_}$	in, see note 2	-BSY signal from SCSI bus to SCSI interface.
C19	s1rst	out	Bus reset signal from SCSI interface to SCSI buffer.
C20	$\overline{s1rst_}$	in, see note 2	-RST signal from SCSI bus to SCSI interface.
E19	$\overline{s1p_}$	inout	Data bus parity
H19	$\overline{s1d7_}$	inout	Data bus
H18	$\overline{s1d6_}$	inout	
G20	$\overline{s1d5_}$	inout	
G19	$\overline{s1d4_}$	inout	
G18	$\overline{s1d3_}$	inout	
F19	$\overline{s1d2_}$	inout	
E20	$\overline{s1d1_}$	inout	
G17	$\overline{s1d0_}$	inout	
A20	s1oe	out	External bus driver direction for $\overline{s1d0_}$ - $\overline{s1d7_}$, $\overline{s0p_}$ signals
B19	$\overline{s1en_}$	out	External driver output enable for $\overline{s1ack_}$, $\overline{s1atn_}$ signals

Table 16-18 SCSI port 1

Bit 7 on the General Port PB, is used as software ID output enable with SCSI interface 1 ($\overline{s1enph_}$). See pb7 in table 16-10 on page 110.

Note 1: If software ID is enabled, the host SCSI ID number is driven to the external logic during arbitration. See documentation about software ID and external buffer solution in Chapter 7, External SCSI Buffers on page 64.

Note 2: The SCSI bus OR-tied signals -SEL, -RST, and -BSY are being generated by the external SCSI buffer, see chapter 7.

16-bits SCSI Interface

When SCSI interface 0 is used in 16-bits wide mode the following signals from SCSI interface 1 are reconfigured to the SCSI interface 0 data bus.

Solder Ball	Name		Direction	Description
	SCSI p1	SCSI-W		
E19	$\overline{s1p_}$	$\overline{s0p1_}$	inout	High data bus parity
H19	$\overline{s1d7_}$	$\overline{s0d15_}$	inout	Data bus bit 15
H18	$\overline{s1d6_}$	$\overline{s0d14_}$	inout	Data bus bit 14
G20	$\overline{s1d5_}$	$\overline{s0d13_}$	inout	Data bus bit 13
G19	$\overline{s1d4_}$	$\overline{s0d12_}$	inout	Data bus bit 12
G18	$\overline{s1d3_}$	$\overline{s0d11_}$	inout	Data bus bit 11
F19	$\overline{s1d2_}$	$\overline{s0d10_}$	inout	Data bus bit 10
E20	$\overline{s1d1_}$	$\overline{s0d9_}$	inout	Data bus bit 9
G17	$\overline{s1d0_}$	$\overline{s0d8_}$	inout	Data bus bit 8
A20	s1oe	s1oe	out	External bus driver direction for $\overline{s1d7_}$ - $\overline{s1d0_}$, s1p_ signals
J17	s1bsy	-	out	Software ID high bit output, <i>see note after 16-17</i>

Table 16-19 16-bits SCSI Interface

ATA

Solder Ball	Name	Direction	Description
V20	iordy	in	I/O ready
R18	dmarq3	in	Request for transfer using DMA handshaking
T20	dmarq2	in	
T19	dmarq1	in	
T18	dmarq0	in	
P17	cs0_	out	Chip select
R19	cs1_	out	Chip select
P20	a2	out	Register address
K20	a1	out	
R20	a0	out	
E18	dmack3_	out	Acknowledge when using DMA handshaking
D20	dmack2_	out	
E19	dmack1_	out	
N18	dmack0_	out	
H19	d15	inout	Data
H18	d14	inout	
G20	d13	inout	
G19	d12	inout	
G18	d11	inout	
F19	d10	inout	
E20	d9	inout	
G17	d8	inout	
N19	d7	inout	
N20	d6	inout	
M17	d5	inout	
M18	d4	inout	
M19	d3	inout	
L19	d2	inout	
L18	d1	inout	
L20	d0	inout	
H20	dior3_	out	Read
B19	dior2_	out	
K19	dior1_	out	
P19	dior0_	out	
J18	intrq3	in	Interrupt request
J19	intrq2	in	
J20	intrq1	in	
K18	intrq0	in	
J17	diow3_	out	Write
C18	diow2_	out	
B20	diow1_	out	
C19	diow0_	out	
A20	ext_oe	out	Output enable for external driver

Table 16-20 ATA

Parallel Port 0

Solder Ball	Name	Direction	Description
V20	p0perror_	in	Error
T18	p0ack_	in	Acknowledge
T19	p0busy	in	Busy
T20	p0fault_	in	Fault
R18	p0select	in	Select
P17	p0data_oe	out	Data output enable
R19	p0selectin_	out	Select in
R20	p0autofd_	out	Autofeed
K20	p0strobe_	out	Strobe
P20	p0init_	out	Initialization
N19	p0d7	inout	Data bus
N20	p0d6	inout	
M17	p0d5	inout	
M18	p0d4	inout	
M19	p0d3	inout	
L19	p0d2	inout	
L18	p0d1	inout	
L20	p0d0	inout	

*Table 16-21 Parallel port 0***Parallel Port 1**

Solder Ball	Name	Direction	Description
D20	p1perror_	in	Error
E18	p1ack_	in	Acknowledge
D19	p1busy	in	Busy
E17	p1fault_	in	Fault
C20	p1select	in	Select
C19	p1data_oe	out	Data output enable
B20	p1selectin_	out	Select in
C18	p1autofd_	out	Autofeed
J17	p1strobe_	out	Strobe
A20	p1init_	out	Initialization
H19	p1d7	inout	Data bus
H18	p1d6	inout	
G20	p1d5	inout	
G19	p1d4	inout	
G18	p1d3	inout	
F19	p1d2	inout	
E20	p1d1	inout	
G17	p1d0	inout	

Table 16-22 Parallel port 1

Shared RAM and Shared RAM-W

8-bit Shared RAM interface:

Solder Ball	Name	Direction	Description
T18	pr_adr1	in	Address bit 1, internally multiplexed with internally generated address bits
V20	pr_adr0	in	Address bit 0, internally multiplexed with internally generated address bits
T19	intio_	in	Interrupt from peripheral
T20	rd_wr	in	Read/write select, a low signal denotes write
R18	pr_req_	in	Request
P17	pr_int_	out	Interrupt to peripheral
R19	pr_ack_	out	Acknowledge
R20	a_sel	out	Address select for externally multiplexed address bits. Low for address from external device.
N19	pr_d7	inout	Data bus
N20	pr_d6	inout	
M17	pr_d5	inout	
M18	pr_d4	inout	
M19	pr_d3	inout	
L19	pr_d2	inout	
L18	pr_d1	inout	
L20	pr_d0	inout	

Table 16-23 8bit Shared RAM

8 bits Shared RAM extended to 16 bits (only applicable together with Shared RAM):

Solder Ball	Name	Direction	Description
H19	pr_d15	inout	Data bus
H18	pr_d14	inout	Data bus
G20	pr_d13	inout	Data bus
G19	pr_d12	inout	Data bus
G18	pr_d11	inout	Data bus
F19	pr_d10	inout	Data bus
E20	pr_d9	inout	Data bus
G17	pr_d8	inout	Data bus

Table 16-24 Shared RAM extended to 16 bits

Serial Ports 2 and 3

Solder Ball	Name	Direction	Description
P19	$\overline{\text{rts2}}$	out	Request to send, serial port 2
K19	txd2	out	Transmit data, serial port 2
K18	$\overline{\text{cts2}}$	in	Clear to send, serial port 2
J20	rxd2	in	Receive data, serial port 2
J19	$\overline{\text{cts3}}$	in	Clear to send, serial port 3
J18	rxd3	in	Receive data, serial port 3
B19	$\overline{\text{rts3}}$	out	Request to send, serial port 3
H20	txd3	out	Transmit data, serial port 3

Table 16-25 Serial ports 2 and 3

Note: The default values of the output signal txd for serial ports 2 and 3 does not comply with the TIA/EIA-232-F serial interface standard. For a complete list of the output default values of the multiplexed interfaces see table 16-16 on page 114.

16.2 DC ELECTRICAL SPECIFICATIONS

16.2.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{DD}	DC supply voltage	-0.3	3.9	V
V _{in}	DC input voltage	-1.0	6.5	V
V _{out}	DC off-state output voltage	-1.0	6.5	V
T _{stg}	Storage temperature	-40	125	°C
T _A	Operating temperature	-40	100	°C

Table 16-26 Absolute Maximum Ratings

ESD protection: ESD protection up to 2kV (Human Body Model according to MIL-STD-883 method 3015).

Lead temperature: According to the specification of JEDEC Level 3 package.

16.2.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	DC supply voltage	3.0	3.3	3.6	V
V _{in}	DC input voltage	-0.5	-	5.5	V
V _{out}	DC off-state output voltage	-0.5	-	5.5	V
T _A	Operating temperature	0	-	70	°C
I _{OH}	High level output current:				
	pa0, pa1, pa2, pa3, pa4, pa5, pa6, pa7 All other	-	-	-12 -4	mA mA
I _{OL}	Low level output current:				
	pa0, pa1, pa2, pa3, pa4, pa5, pa6, pa7 All other	-	-	12 4	mA mA

Table 16-27 Recommended Operating Conditions

16.2.3 DC Electrical Characteristics

Symb ol	Parameter	Min	Typ	Max	Unit
V_{IH}	High level input voltage, all inputs except clkin	2.0	-	5.5	V
V_{IL}	Low level input voltage, all inputs except clkin	-0.5	-	0.8	V
V_{IH}	High level input voltage, clkin	$0.7 \cdot V_{DD}$	-	5.5	V
V_{IL}	Low level input voltage, clkin	-0.5	-	$0.3 \cdot V_{DD}$	V
	Schmitt Trigger Hysteresis (see table 16-30)	0.6	0.7	-	V
V_{OH}	High level output voltage	2.4	-	V_{dd}	V
V_{OL}	Low level output voltage	-	-	0.4	V
I_{in}	Input leakage current	-10	-	10	μA
I_{ioz}	I/O leakage current				
	$V_{in} < V_{DD}$	-10	-	10	μA
	$V_{DD} < V_{in} < 5.5V$	-200	-	200	μA
I_{DD}	Supply current	-	115	210	mA

Table 16-28 DC Electrical Characteristics

16.2.4 Input Buffer Types

Signal	Buffer Type
clkin	CMOS
Input: $\overline{cts0_}$, $\overline{irq_}$, $\overline{nmi_}$, $\overline{reset_}$, rxd0 Inout: mdio, pa0, pa1, pa2, pa3, pa4, pa5, pa6, pa7, pb1, pb2, pb3, pb4, pb5, pb6, pb7	TTL Schmitt Trigger
All other	TTL

Table 16-29 Input Buffer Types

16.3 AC ELECTRICAL SPECIFICATIONS

This section provides the AC characteristics for the ETRAX 100. The timing sequences are related to the internal 100 MHz clock.

Table 16-30 Bus State Descriptions lists all bus states used in the timing diagrams on the following pages.

Bus State Descriptions

State	Description	Comment
T _a	Activate state. RD, WR or INTA strobes are asserted in this state. CAS is asserted after the end of this state.	
T _d	Data state. 'Data in' is sampled at the end of this state, except for EDO DRAM read, where data is sampled 15 ns after the end of this state.	
T _z	Data bus turn-off state. This state is inserted between bursts to allow ETRAX 100 and external units to turn off their outputs before the data bus is driven by another source. This state may overlap with a T _{ew} state.	
T _{pa}	RAS precharge activate state. RAS is set high after the end of this state.	
T _{pd}	RAS precharge state. DRAM row address is asserted after the end of this state. During DRAM refresh, CAS is set low after the end of this state.	
T _{ra}	RAS activate state. RAS is set low after the end of this state.	
T _{rd}	Row address hold state.	
T _{be0} , T _{be1}	Burst end states. Inserted at the end of an EDO DRAM read burst, to allow the last data of the burst to be sampled. These states may overlap with a T _{ew} state.	
T _{ew}	Early wait state. This state may overlap with a T _z , T _{zw} , T _{be0} or T _{be1} state.	Inserted before T _a
T _{lw}	Late wait state.	Inserted between T _a and T _d
T _{zw}	Turn-off wait state. This state may overlap with a T _{ew} state.	Inserted after T _d
T _{xw}	External wait state.	
T _{xx}	Any bus state.	

Table 16-30 Bus State Descriptions

Wait States

Table of wait state parameters used in these diagrams. These parameters correspond to the wait state values described in chapter 15.

Name	Description
ew	Number of early wait states.
lw	Number of late wait states.
zw	Number of turn-off wait states.
c	$\overline{\text{CAS}}$ delay.
cw	Number of $\overline{\text{CAS}}$ wait states.
cp	Number of $\overline{\text{CAS}}$ precharge wait states.
rp	Number of $\overline{\text{RAS}}$ precharge wait states.
rs	Number of row address setup wait states.
rh	Number of row address hold wait states.
cz	Number of turn-off wait states after $\overline{\text{CAS}}$.

Table 16-31 Wait States

16.3.1 SRAM/flash/peripheral Timing

Read cycle

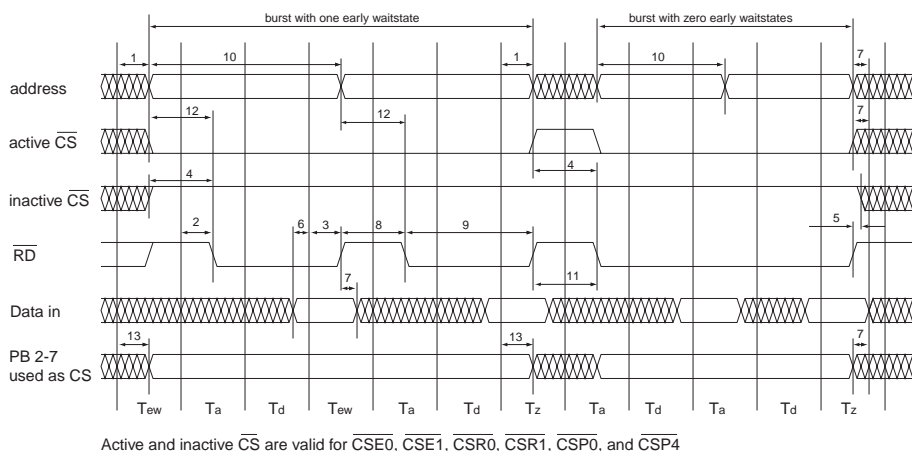


Figure 16-2 SRAM/flash/peripheral read cycle

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock. See note.	2	-	8	-	ns
2	t_{rl}	Read fall delay from clock	2	-	8	-	ns
3	t_{rh}	Read rise delay from clock	2	-	7	-	ns
4	t_{cshr}	Chip select high to read low	8	-	-	-	ns
5	t_{rhcs}	Read high to chip select low	0	-	-	-	ns
6	t_{ds}	Data in setup time to clock	0	-	-	-	ns
7	t_{dh}	Data hold time from addr, chip select or read, whichever occurs first	0	-	-	-	ns
8	t_{rhw}	Read inactive width within burst	-2	-	-	10-ew	ns
9	t_{rw}	Read active width	16	20	-	10-lw	ns
10	t_{rc}	Read cycle	-	20	-	10-(ew+lw)	ns
11	t_{rhr}	Read inactive width after burst	8	-	-	10-zw	ns
12	t_{ar}	Read inactive time after chip select or address	-2	-	-	10-ew	ns
13	t_{pcs}	PB delay from clock when used as chip selects	3	-	12	-	ns

Table 16-32

Note: Valid for $\overline{CSE0}$, $\overline{CSE1}$, $\overline{CSR0}$, $\overline{CSP0}$ and $\overline{CSP4}$.

Write cycle, normal write

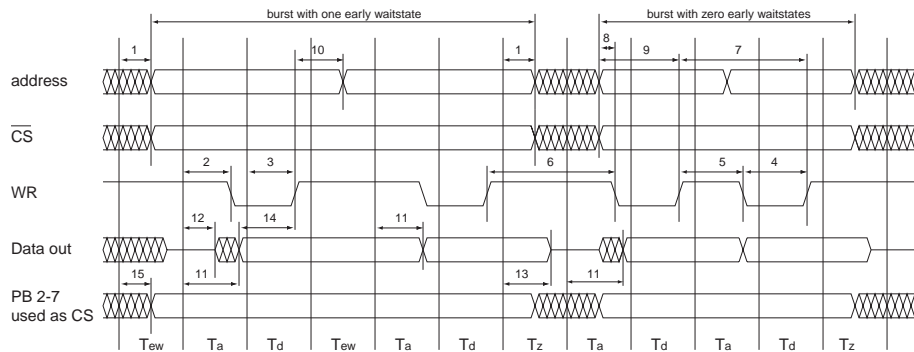


Figure 16-3 SRAM/flash/peripheral write cycle, normal write

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock	2	-	8	-	ns
2	t_{wl}	Write low delay from clock	7	-	13	-	ns
3	t_{wh}	Write high delay from clock	7	-	11	-	ns
4	t_{ww}	Write pulse width	6	-	-	10·lw	ns
5	t_{whw}	Write inactive width within burst	9	-	-	10·ew	ns
6	t_{whl}	Write inactive width after burst	19	-	-	10·zw	ns
7	t_{wc}	Write cycle time		20	-	10·(ew+lw)	ns
8	t_{awl}	Address and chip select setup to write low	2	-	-	10·ew	ns
9	t_{awh}	Address and chip select setup to end of write	11	-	-	10·(ew+lw)	ns
10	t_{ahw}	Address hold after write high	3	-	-	-	ns
11	t_{do}	Data delay from clock	6	-	13	-	ns
12	t_{doe}	Data turn on time from clock	6	-	-	-	ns
13	t_{doz}	Data turn off time from clock	6	-	10	10·zw	ns
14	t_{dwh}	Data valid to end of write	6	-	-	10·lw	ns
15	t_{pcs}	PB delay from clock, when used as chip selects	3	-	12	-	ns

Table 16-33

Write cycle, extended write

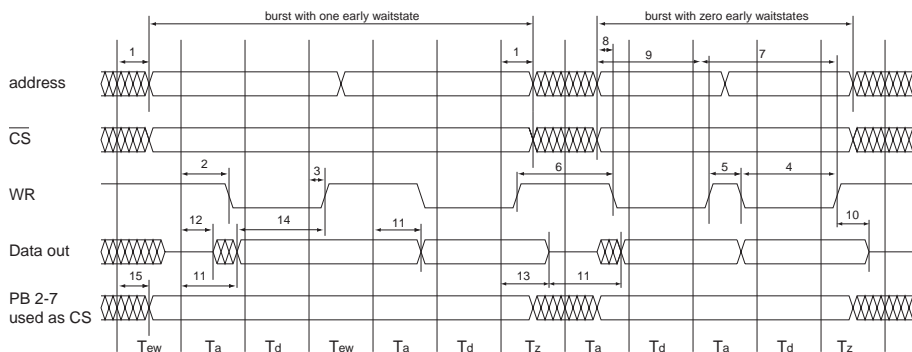


Figure 16-4 SRAM/flash/peripheral write cycle, extended write

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address and chip select delay from clock	2	-	8	-	ns
2	t_{wl}	Write low delay from clock	7	-	13	-	ns
3	t_{whx}	Write high delay from clock	2	-	7	-	ns
4	t_{wwx}	Write pulse width	11	-	-	10·lw	ns
5	t_{whwx}	Write inactive width within burst	4	-	-	10·ew	ns
6	t_{whlx}	Write inactive width after burst	13	-	-	10·zw	ns
7	t_{wcx}	Write cycle time	-	20	-	10·(ew+lw)	ns
8	t_{awl}	Address and chip select setup to write low	2	-	-	10·ew	ns
9	t_{awhx}	Address and chip select setup to end of write	16	-	-	10·(ew+lw)	ns
10	t_{whdx}	Data hold after end of write	2	-	-	10·ew within burst, 10·zw after burst	ns
11	t_{do}	Data delay from clock	6	-	13	-	ns
12	t_{doe}	Data turn on time from clock	6	-	-	-	ns
13	t_{doz}	Data turn off time from clock	6	-	10	10·zw	ns
14	t_{dwhx}	Data valid to end of write	11	-	-	10·lw	ns
15	t_{pcs}	PB delay from clock, when used as chip selects	3	-	12	-	ns

Table 16-34

16.3.2 DRAM

Fast page mode, read

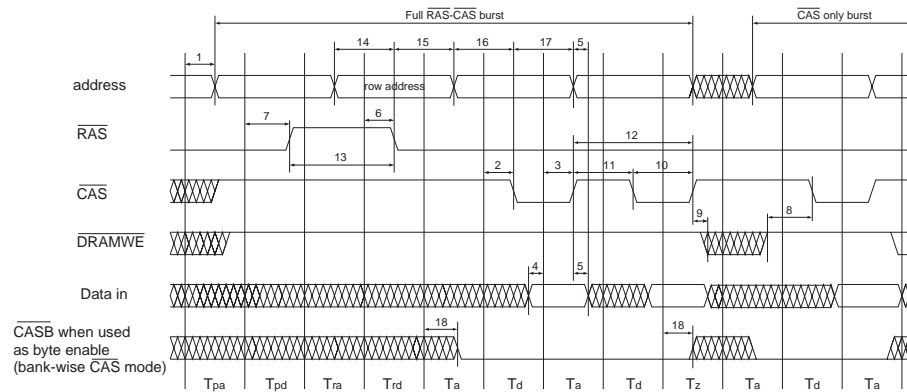


Figure 16-5 DRAM, fast page mode, read

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock	2	-	8	-	ns
2	t_{casl}	$\overline{\text{CAS}}$ fall delay from clock	2	-	8	5-c	ns
3	t_{cash}	$\overline{\text{CAS}}$ rise delay from clock	2	-	8	-	ns
4	t_{ds}	Data in setup time to clock	0	-	-	-	ns
5	t_{dh}	Data in hold time from $\overline{\text{CAS}}$ or address change, whichever occurs first	0	-	-	-	ns
6	t_{rasl}	$\overline{\text{RAS}}$ fall time from clock	3	-	10	-	ns
7	t_{rash}	$\overline{\text{RAS}}$ rise time from clock	8	-	13	-	ns
8	t_{rcs}	$\overline{\text{DRAMWE}}$ high setup time to $\overline{\text{CAS}}$ low	4	-	-	5-c	ns
9	t_{rch}	$\overline{\text{DRAMWE}}$ high hold time from $\overline{\text{CAS}}$ high	2	-	-	-	ns
10	t_{cas}	$\overline{\text{CAS}}$ pulse width	7	-	-	10-cw - 5-c	ns
11	t_{cp}	$\overline{\text{CAS}}$ precharge time	7	-	-	10-cp + 5-c	ns
12	t_{pc}	$\overline{\text{CAS}}$ cycle time	-	20	-	10-(cp + cw)	ns
13	t_{rp}	$\overline{\text{RAS}}$ precharge time	14	-	-	10-(rp + rs)	ns
14	t_{asr}	Row address setup time to $\overline{\text{RAS}}$	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from $\overline{\text{RAS}}$	4	-	-	10-rh	ns
16	t_{asc}	Column address setup time to $\overline{\text{CAS}}$	7	-	-	10-cp + 5-c	ns
17	t_{cah}	Column address hold time from $\overline{\text{CAS}}$	7	-	-	10-cw - 5-c	ns
18	t_{be}	$\overline{\text{CASB}}$ delay from clock, when used as byte enable (bankwise CAS mode)	2	-	8	-	ns

Table 16-35

EDO DRAM, read

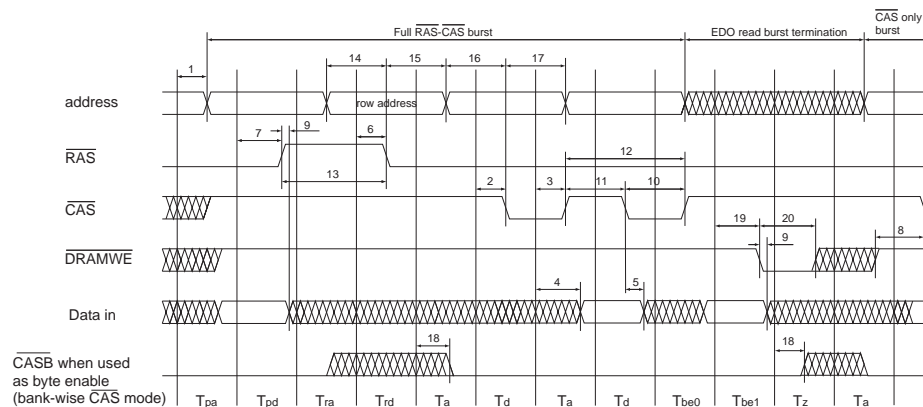


Figure 16-6 EDO DRAM, read

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock	2	-	8	-	ns
2	t_{casl}	$\overline{\text{CAS}}$ fall delay from clock	2	-	8	5-c	ns
3	t_{cash}	$\overline{\text{CAS}}$ rise delay from clock	2	-	8	-	ns
4	t_{dd}	Data in valid delay from clock	-	-	15	-	ns
5	t_{coh}	Data in hold time from $\overline{\text{CAS}}$ low	4	-	-	$(-10) \cdot \text{cp} - 5 \cdot \text{c}$	ns
6	t_{rasl}	$\overline{\text{RAS}}$ fall time from clock	3	-	10	-	ns
7	t_{rash}	$\overline{\text{RAS}}$ rise time from clock	8	-	13	-	ns
8	t_{rcs}	$\overline{\text{DRAMWE}}$ high setup time to $\overline{\text{CAS}}$ low	4	-	-	5-c	ns
9	t_{dh}	Data in hold time from $\overline{\text{DRAMWE}}$ low or $\overline{\text{RAS}}$ high, whichever occurs first.	0	-	-	-	ns
10	t_{cas}	$\overline{\text{CAS}}$ pulse width	7	-	-	$10 \cdot \text{cw} - 5 \cdot \text{c}$	ns
11	t_{cp}	$\overline{\text{CAS}}$ precharge time	7	-	-	$10 \cdot \text{cp} + 5 \cdot \text{c}$	ns
12	t_{pc}	$\overline{\text{CAS}}$ cycle time	-	20	-	$10 \cdot (\text{cp} + \text{cw})$	ns
13	t_{rp}	$\overline{\text{RAS}}$ precharge time	14	-	-	$10 \cdot (\text{rp} + \text{rs})$	ns
14	t_{asr}	Row address setup time to $\overline{\text{RAS}}$	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from $\overline{\text{RAS}}$	4	-	12	10-rh	ns
16	t_{asc}	Column address setup time to $\overline{\text{CAS}}$	7	-	-	$10 \cdot \text{cp} + 5 \cdot \text{c}$	ns
17	t_{cah}	Column address hold time from $\overline{\text{CAS}}$	7	-	-	$10 \cdot \text{cw} - 5 \cdot \text{c}$	ns
18	t_{be}	$\overline{\text{CASB}}$ delay from clock, when used as byte enable (bankwise $\overline{\text{CAS}}$ mode)	2	-	8	-	ns
19	t_{wel}	$\overline{\text{DRAMWE}}$ fall delay from clock	7	-	13	-	ns
20	t_{wew}	$\overline{\text{DRAMWE}}$ pulse width after EDO read burst	7	-	-	$10 \cdot \text{cz}$	ns

Table 16-36

DRAM, write

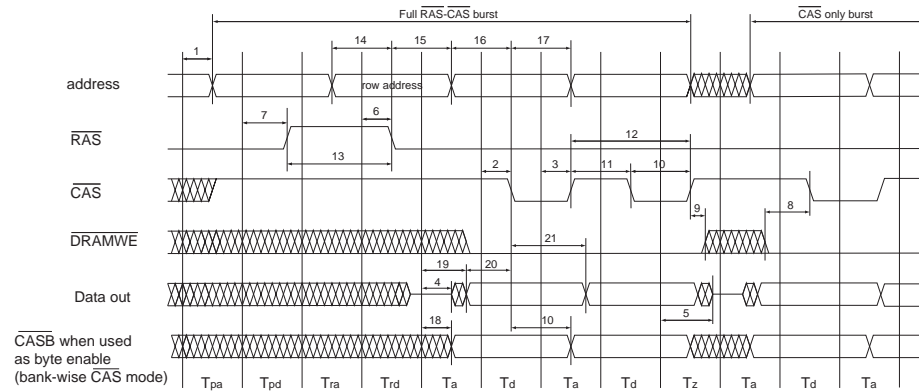


Figure 16-7 DRAM, write

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock	2	-	8	-	ns
2	t_{casl}	$\overline{\text{CAS}}$ fall delay from clock	2	-	8	5-c	ns
3	t_{cash}	$\overline{\text{CAS}}$ rise delay from clock	2	-	8	-	ns
4	t_{doe}	Data out turn on time from clock	7	-	-	-	ns
5	t_{doz}	Data out turn off time from clock	-	-	10	10-cz	ns
6	t_{rasl}	RAS fall time from clock	3	-	10	-	ns
7	t_{rash}	RAS rise time from clock	8	-	13	-	ns
8	t_{wcs}	DRAMWE low setup time to CAS low	2	-	-	-	ns
9	t_{weh}	DRAMWE low hold time from CAS high	1	-	-	-	ns
10	t_{cas}	$\overline{\text{CAS}}$ pulse width	7	-	-	10-cw - 5-c	ns
11	t_{cp}	CAS precharge time	7	-	-	10-cp + 5-c	ns
12	t_{pc}	CAS cycle time	-	20	-	10-(cp + cw)	ns
13	t_{rp}	RAS precharge time	14	-	-	10-(rp + rs)	ns
14	t_{asr}	Row address setup time to $\overline{\text{RAS}}$	9	-	-	10-rs	ns
15	t_{rah}	Row address hold time from $\overline{\text{RAS}}$	4	-	12	10-rh	ns
16	t_{asc}	Column address setup time to $\overline{\text{CAS}}$	7	-	-	10-cp + 5-c	ns
17	t_{cah}	Column address hold time from $\overline{\text{CAS}}$	7	-	-	10-cw - 5-c	ns
18	t_{be}	$\overline{\text{CASB}}$ delay from clock, when used as byte enable (bankwise CAS mode)	2	-	8	-	ns
19	t_{do}	Data delay from clock	6	-	-	-	ns
20	t_{dsc}	Data setup to $\overline{\text{CAS}}$ low	2	-	-	5-c	ns
21	t_{dhc}	Data hold after $\overline{\text{CAS}}$ low	10	-	-	10-cw - 5-c	ns

Table 16-37

CAS before RAS refresh cycle

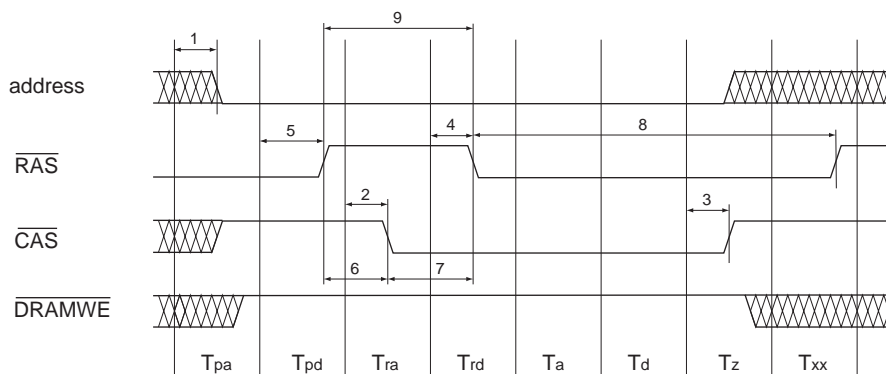


Figure 16-8 CAS before RAS refresh cycle

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t_a	Address delay from clock	2	-	8	-	ns
2	t_{casl}	CAS fall delay from clock	2	-	8	5-c	ns
3	t_{cash}	CAS rise delay from clock	2	-	8	-	ns
4	t_{rasl}	RAS fall time from clock	3	-	10	-	ns
5	t_{rash}	RAS rise time from clock	8	-	13	-	ns
6	t_{rpc}	RAS to CAS precharge time	2	-	-	10·rp	ns
7	t_{csr}	CAS setup time to RAS	7	-	-	10·rs	ns
8	t_{ras}	RAS pulse width	40	-	-	10·(rh + cp + cw)	ns
9	t_{rp}	RAS precharge time	14	-	-	10·(rp + rs)	ns

Table 16-38

16.3.3 General Bus Interface Timing Diagrams

Data turn-off timing

Figure Logic Analyzer Mode and Test specifies the relation of the data turn-off timing of DRAM and non-DRAM bursts.

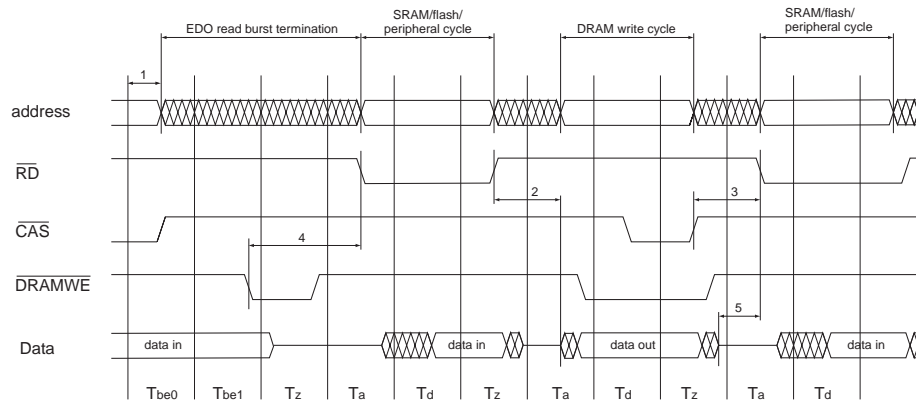


Figure 16-9 Data turn-off timing

No	Name	Explanation	Without waitstates			Add with waitstates	Unit
			Min	Nom	Max		
1	t _a	Address delay from clock	2	-	8	-	ns
2	t _{rdo}	Read high to data out	13	-	-	10-zw	ns
3	t _{cr}	CAS high to read low	7	-	-	10-cz	ns
4	t _{weir}	DRAMWE low to read low after EDO read burst	13	-	-	10-cz	ns
5	t _{dozr}	Data out turn-off before read low	5	-	-	-	ns

Table 16-39

External interrupt acknowledge cycle

The external interrupt acknowledge cycle is always using a maximum number of waitstates.

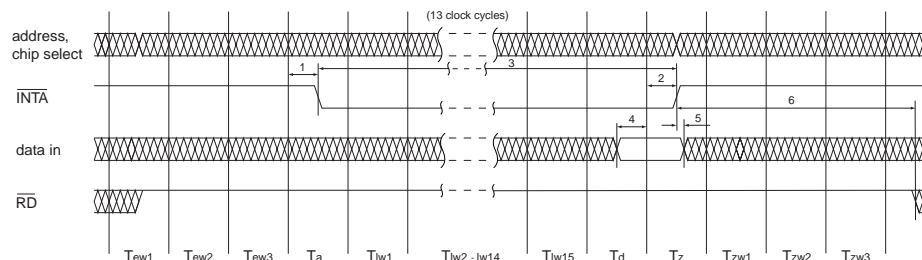
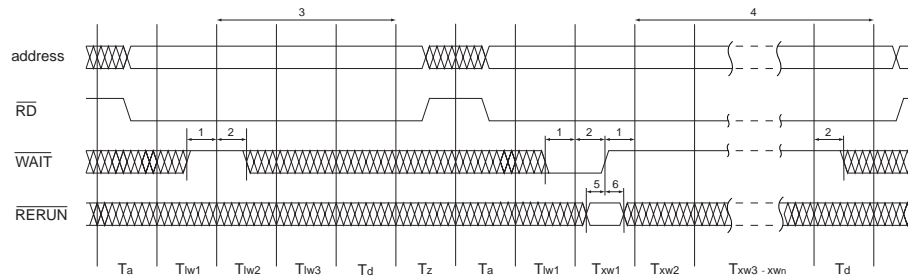


Figure 16-10 External interrupt acknowledge cycle

No	Name	Explanation	Min	Nom	Max	Unit
1	t_{il}	\overline{INTA} low delay from clock	2	-	8	ns
2	t_{ih}	\overline{INTA} high delay from clock	2	-	7	ns
3	t_{iw}	\overline{INTA} pulse width	167	170	172	ns
4	t_{ds}	Data in setup time to clock	0	-	-	ns
5	t_{dh}	Data in hold time from \overline{INTA} high	0	-	-	ns
6	t_{ihr}	\overline{INTA} high to read low	38	-	-	ns

Table 16-40

Wait and rerun timing*Figure 16-11 Wait and rerun timing*

No	Name	Explanation	Min	Nom	Max	Note	Unit
1	t_{xws}	WAIT setup time to clock	0	-	-	Note 1	ns
2	t_{xwh}	WAIT hold time from clock	2	-	-	Note 1	ns
3	t_{xwi}	WAIT sampled to end of bus cycle (WAIT not activated)	30	30	30	Note 2	ns
4	t_{xwa}	WAIT sampled to end of bus cycle (WAIT activated)	50	-	80	Note 2	ns
5	t_{res}	RERUN setup time to WAIT high	1	-	-		
6	t_{reh}	RERUN hold time after WAIT high	1	-	-		ns

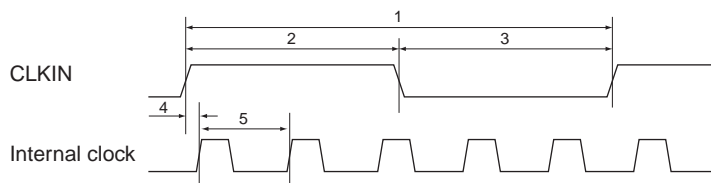
Table 16-41

Note 1: $\overline{\text{WAIT}}$ is synchronized internally. Setup and hold times need to be taken into consideration only if detection in a specific clock cycle is required.

Note 2: $\overline{\text{WAIT}}$ is sampled 3 clock cycles before the end of the bus cycle, taking only the internal wait states into consideration. In order to recognize $\overline{\text{WAIT}}$, a number of internal lw and/or ew waitstates must be added. Typically 3 internal wait states are needed, but this depends on the external wait state logic.

16.3.4 Reset and clock timing

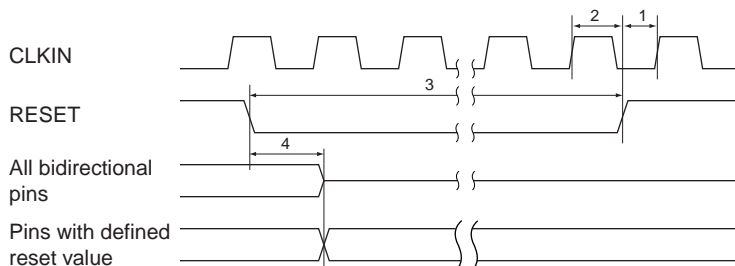
System clock timing



No	Name	Explanation	Min	Nom	Max	Unit
1	t_{clkp}	Input clock period (See note)	49	50	51	ns
2	t_{clkh}	Input clock high time	15	-	-	ns
3	t_{ckl}	Input clock low time	15	-	-	ns
4	t_{ckld}	Input clock to internal clock delay	2	3.5	5	ns
5	t_{ckp}	Internal clock period	-	$0.2 \cdot t_{clkp}$	-	ns

Note: Some applications may require less tolerance on the clock period. For example: if txer is configured as the clock for Fast Ethernet a greater accuracy of the clock cycle is needed (see 100BASE-T standard: IEEE 802.3u.).

Reset timing



No	Name	Explanation	Min	Nom	Max	Unit
1	t_{ress}	RESET setup to clkin (See note)	2	-	-	ns
2	t_{resh}	RESET hold from clkin (See note)	0	-	-	ns
3	t_{resw}	RESET pulse width	$5 \cdot t_{clkp}$	-	-	ns
4	t_{resd}	RESET to output delay	-	-	25	ns

Note: Reset is internally synchronized. Setup and hold times can be ignored unless recognition on a specific clock cycle is required.

16.4 PHYSICAL DIMENSIONS

The package of the ETRAX 100 is a 256 lead Plastic Ball Grid Array, PBGA.

256 PBGA
Plastic Ball Grid Array Package - Mechanical Drawing

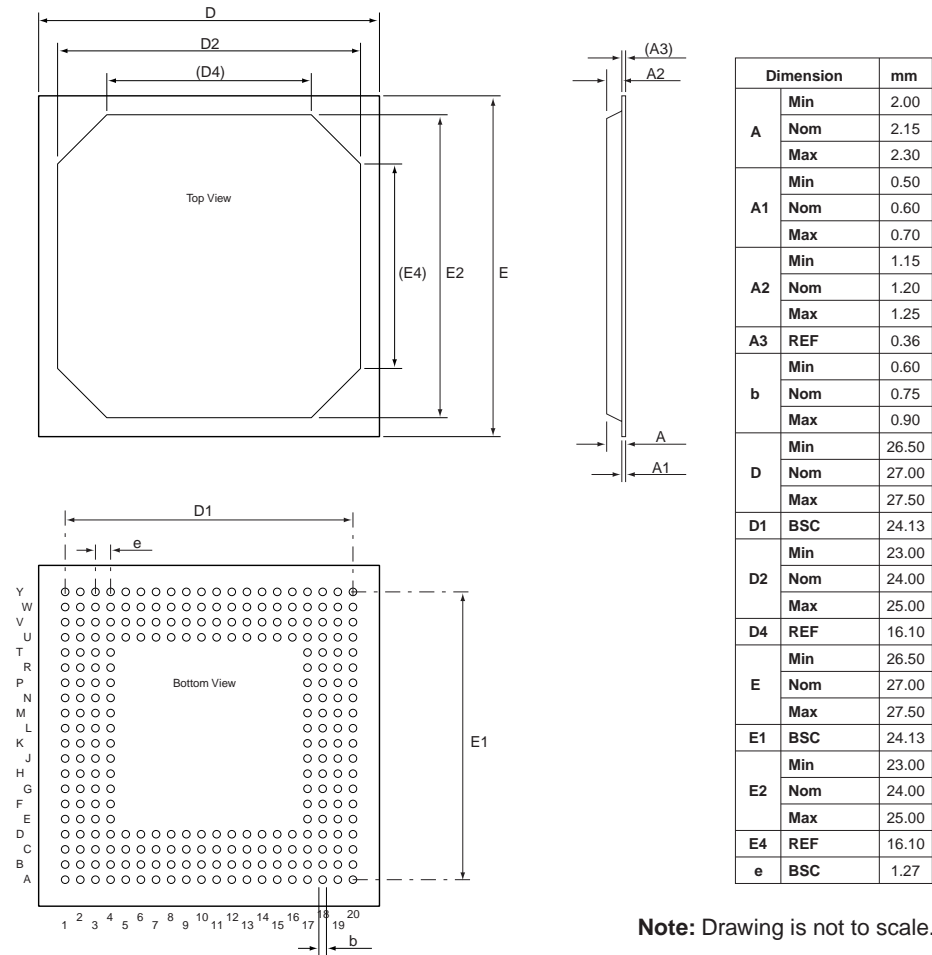


Figure 16-12 256 PBGA - Mechanical drawing