
APPENDIX A LOGIC ANALYZER SUPPORT

The use of the internal cache memory makes it impossible to directly monitor the program execution with e.g. a logic analyzer. The built-in logic analyzer support is a way to get around this problem. The principle is to let two extra ETRAX 100 chips run in parallel with the Device Under Test (DUT). These extra chips, called Monitor Chips (MC), listen to the data bus and some other signals from the DUT. Because the MC:s run in parallel with the DUT from reset, their internal CPU and cache states are identical with those of the DUT.

The MC:s will run in a special monitor mode, where some of the pins are used to output the internal CPU data and address buses, and status information. These pins can then be monitored by a logic analyzer.

One MC is the Data Monitor (DMC), that outputs the CPU data and CPU status. The other one is the Address Monitor (AMC), that outputs the CPU address and the cache status.

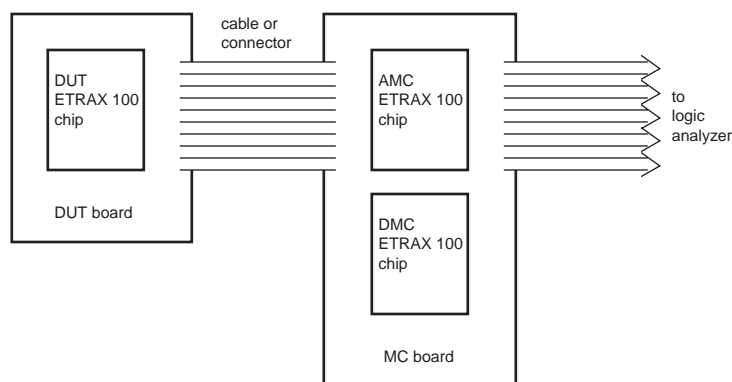


Figure A-13 Block diagram

