
APPENDIX C PLL CLOCK GENERATION

ETRAX 100 uses a PLL to generate the internal reference clock from the clock supplied at the `clkin` pin. The PLL circuit multiplies the `clkin` frequency by a factor of 10. For normal operation the `clkin` frequency should be 20 MHz, resulting in an internal reference frequency of 200 MHz.

At reset the internal reference clock is disabled as long as reset is active. When reset is released the reference clock is disabled for an additional time of 1.6 ms. During this time the PLL locks the internal reference signal to the `clkin` signal.

Pin usage

The PLL in ETRAX 100 uses the following pins:

Pin	Direction	Description
<code>clk_{in}</code>	In	External clock input.
<code>pll_{agn}</code>	Out	Analog ground output that provides the reference ground for the loop filter. It should only be connected to the RC network in the loop filter, see below
<code>pll_{p2}</code>	Out	Charge Pump output to external loop filter. Voltage at this pin control VCO frequency.
<code>pll_{vdd}</code>	In	PLL power, 3.3 V.
<code>pll_{vss}</code>	In	PLL ground.

Table 16-42 PLL pin usage

PLL Power Connection

The power connections for the PLL, `pllvdd` and `pllvss`, should be separated from the power and ground for the rest of the ETRAX 100 chip. The noise level on `pllvdd` should be kept to less than 10mV.

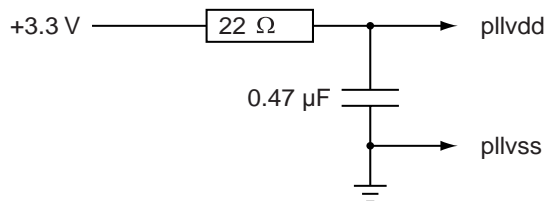


Figure 16-14 Sample noise filter for pll_{vdd}.

External loop Filter

The loop filter resistor and capacitor should be connected as close as possible to the asic.

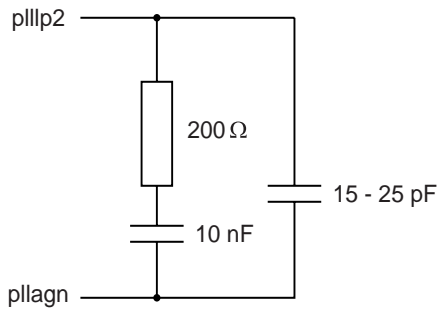


Figure 16-15 External loop filter