

# AXIS ETRAX FS

## *A Flexible Multi-Processor System-on-Chip for Network Devices*

The ETRAX FS is a powerful system-on-chip enabling design of high-performance and price competitive embedded devices running the latest Linux kernels. It integrates a powerful CPU, device interfaces, two Ethernet (10/100) controllers, MMU, on-chip RAM and a flexible I/O protocol processor for device attachment. It is highly suited for use in a wide range of embedded applications such as industrial automation controllers, access control, security equipment, data acquisition etc. Axis offers the whole suite of development tools required for rapid hardware and software development; reference designs, a well established Linux SDK, debugging tools as well as qualified engineering support.

### High Performance with Low Power Consumption

The 200MHz 32-bit RISC ISA enables compact code and exceptional price/performance with low power consumption. On-chip 16 KB I-cache and 16 KB D-cache takes full advantage of the CPU performance.

### Designed for Networking

Dual 10/100 Mbit/s full duplex Ethernet MAC together with hardware support for IP checksum calculation makes the ETRAX FS ideal for networking high performance devices.

### I/O Protocol Processor for Flexible Device Attachment

The patented micro-code programmable I/O processor consists of three 200 MHz 32-bit processors with local memory and hardware accelerators. It has real time performance, capable of running at least two I/O protocols simultaneously.

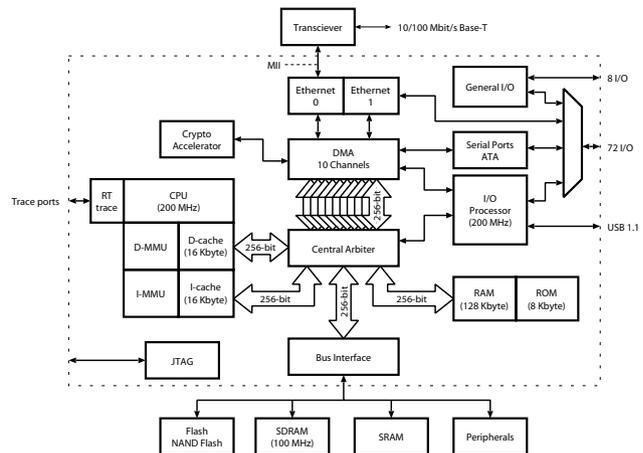


- Designed for Linux with a powerful 200MHz CPU including an MMU for real Linux support
- Hardware crypto accelerator supporting wire-speed cryptography
- Built in memory controller supporting SDRAM, SRAM, EPROM, EEPROM and NOR/NAND Flash PROM without external logic
- Integrated I/O controller for Ethernet, synchronous serial ports and ATA.
- Linux 2.6 kernel source code and free development tools available

Specifications

32-Bit RISC CPU	200 MHz RISC CPU with a 32-bit data and address width 16-bit instruction set optimized for compact code Instruction pre-fetch and dynamic branch prediction A 256-bit wide system bus. 5-stage pipeline 1-cycle multiplication. User and kernel mode for protected memory access
Memory Management Unit (MMU)	Separate instruction and data MMU featuring 4 GB of virtual uniform address space for each user process Address space protection Supports zero-copy shared memory schemes and includes two 64-entry Translation Look-aside buffers
Cache Memory	Multi-processor enabled I-and D-cache Each cache is 16 KB and 2-way set associative and has a 256-bit interface to the system bus for high internal bandwidth Snooping cache coherence mechanism (MESI protocol)
Central Arbiter	Memory arbitration providing non-blocking access to internal memory during external memory accesses 1.6 GB/s peak internal throughput
Internal RAM	128 KB and 256-bit wide RAM with 20 ns cycle time
I/O Processor	One master and two slave 32-bit processors running at 200 MHz. Access to internal system bus and DMA Local memory Function blocks also available to main CPU are clock generators, timers, trigger logic, hardware acceleration of CRC Capable of micro code based implementation of at least two I/O protocols simultaneously. Controls 72 100 MHz I/O pins Can be programmed to support parallel and serial ports, PC-Card/CardBus/PCI, USB 2.0 FS/HS host and device, SCSI-2/SCSI-3, ATA PIO mode 4(8 MB/s)/Multiword DMA mode 2 (16 MB/s)/UltraDMA mode 2 and 5 (33 and 100 MB/s), and proprietary interfaces.
Crypto Accelerator	Configurable, hardware accelerated DES, 3DES, AES, MD5, SHA-1, and IP checksum calculation for data cryptography, 2*100 Mbit/s Equally efficient serial or parallel configuration of up to three algorithms.
Direct Memory Access (DMA)	10 DMA channels each with 64 bytes FIFO for low latency and high throughput data transfers to and from internal and external units 400 MB/s peak bandwidth per DMA channel. Support for real time clients through multiple virtual channels concept with fast channel switching
Dual Ethernet Controller's	Dual 10/100 Mbit/s Ethernet MAC (compatible with IEEE 802.3 and Fast Ethernet standards)
4 Asynchronous Serial Ports	Full buffering and parity control. One handshake signal in each direction. Supports polled, interrupt driven and DMA controlled operation. Independent RX and TX operation. Support baud rates from 56.25 baud to 12.5 Mbaud
2 Synchronous Serial Ports	I2S master and slave mode with internal and external clock. Universal SPI interface up to 16.67 MHz; some modes up to 50 MHz. Partial I2C support. Compatible with many generic synchronous serial protocols. Supports IEC 60958 mode. Up to 50 MHz internal clock generator. Up to 100 Mbit/s transmission and 300 Mbit/s reception in chip-to-chip mode
ATA	Single ATA controller. Support for PIO mode 4 (8 MB/s), Multiword DMA mode 2 (16 MB/s) and UltraDMA mode 2 (33 MB/s). Configuration of up to 4 ATA ports for up to 8 IDE drives

USB PHY Port	One FS/LS USB PHY port accessible from the I/O processor. Support for host and device mode
External Bus Interface and Memory Controllers	Memory controllers for SDRAM (100 MHz), SRAM, EPROM, parallel EEPROM, NOR/NAND flash PROM. Bus width configurable to 16 or 32 bits. Support for 64-bit SDRAM DIMM and SO-DIMM modules
Slave Mode	Support for allowing an external chip (bus master) to read and write mode registers and internal memory. While in slave mode, the chip looks like an I/O device to the external bus master
Timers and Watchdog	Two programmable 32-bit timers with selectable input clock frequencies 8-bit counter able to count wraps for the 32-bit counters One fixed 32-bit read only counter. Watchdog timer
General Purpose Ports	80 read/write configurable I/O pins (multiplexed with other I/O functions). 8 pins can be configured as inputs for interrupts
Clock Generator	Internal 200 MHz operating frequency, generated by a PLL from an external 12 MHz clock signal
Interrupt Control	Vectorized interrupt; internal (I/O ports, network interface, DMA, and timer) and external (IRQ and NMI)
On-Chip Debug	In circuit debug with JTAG interface requiring no functional SW on the target Hardware watchpoints, breakpoints and single step. Real-time execution path tracing via dedicated high-speed I/O
Software and Development Tools	Linux kernel and device drivers, GNU tool chain including compiler, debugger and other tools, and documentation are available free of charge from: <a href="http://developer.axis.com">developer.axis.com</a>
Bootstrap Program Download	Supports initial loading to internal RAM from NOR/NAND flash PROM, serial port, and network. Code loaded to internal RAM can be designed to enable download of program to initially empty Flash PROM, or other external memory
Package	256 pin Plastic Ball Grid Array. 27x27 mm
Operating Conditions	Supply voltage core: 1.4 - 1.6 V Supply voltage I/O: 3.0 - 3.6 V Ambient temperature range: 0 - 85 °C Power consumption: 465 mW



For more information, visit: <http://developer.axis.com>