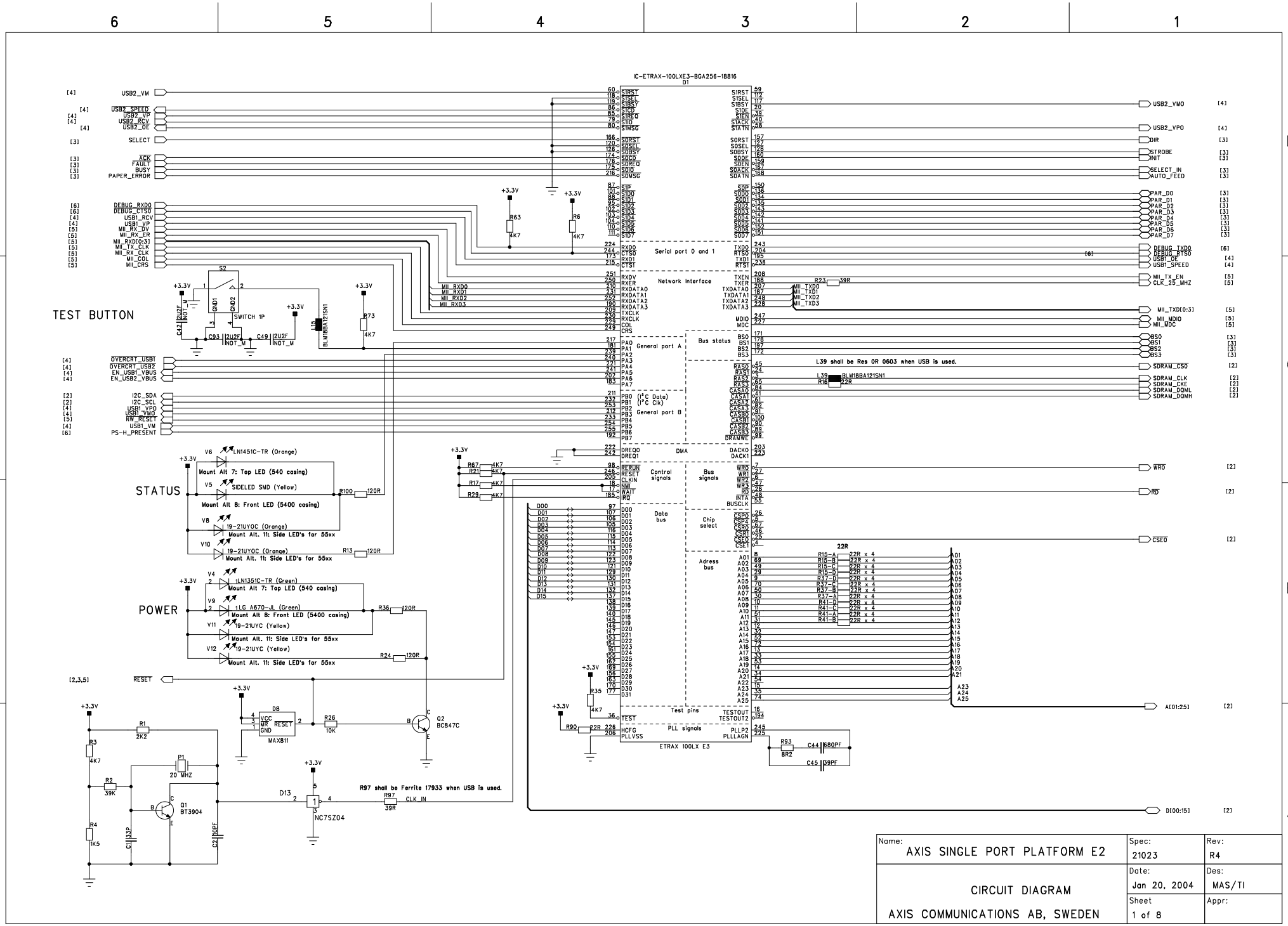
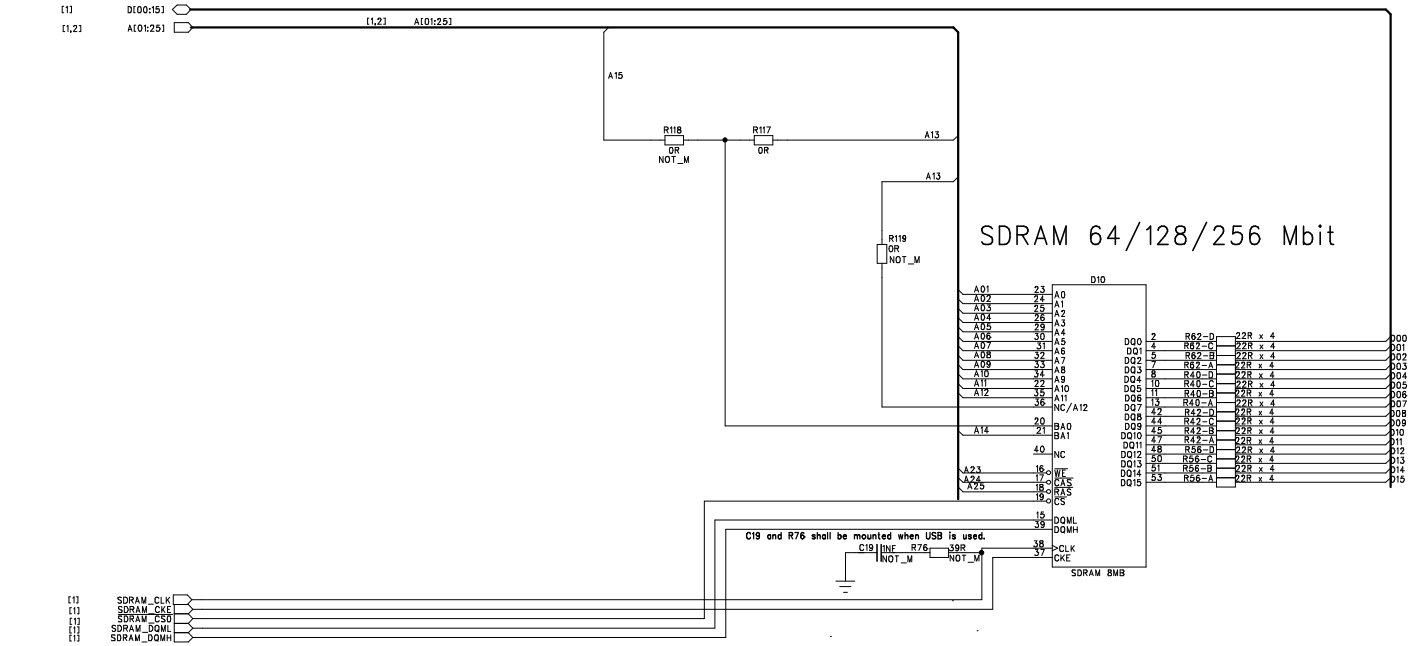
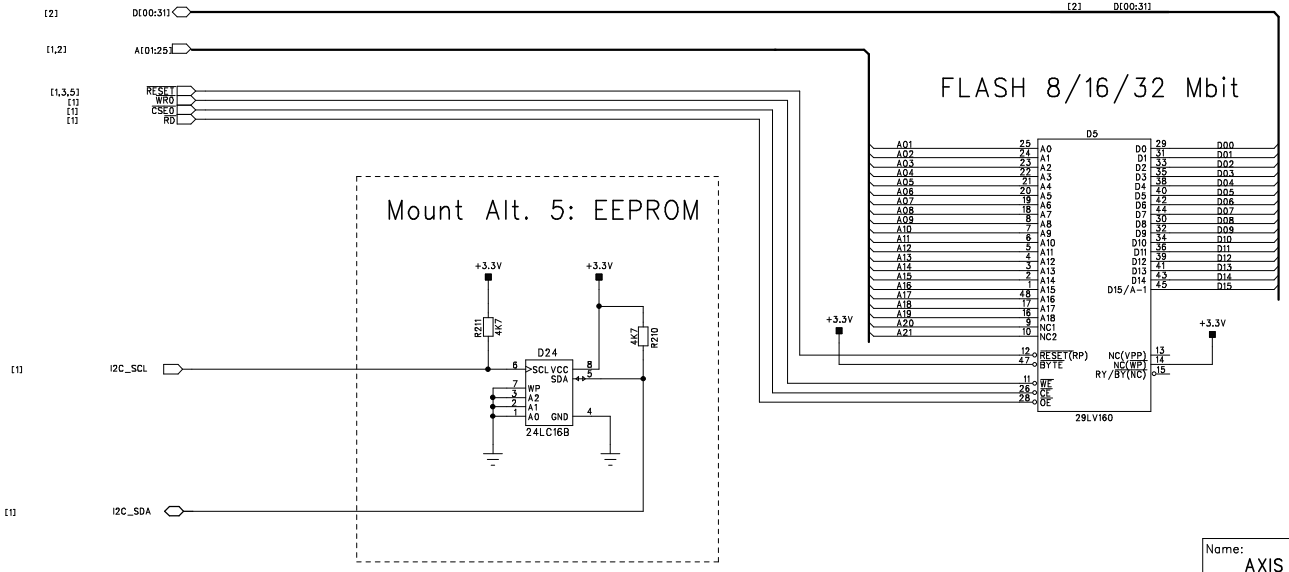
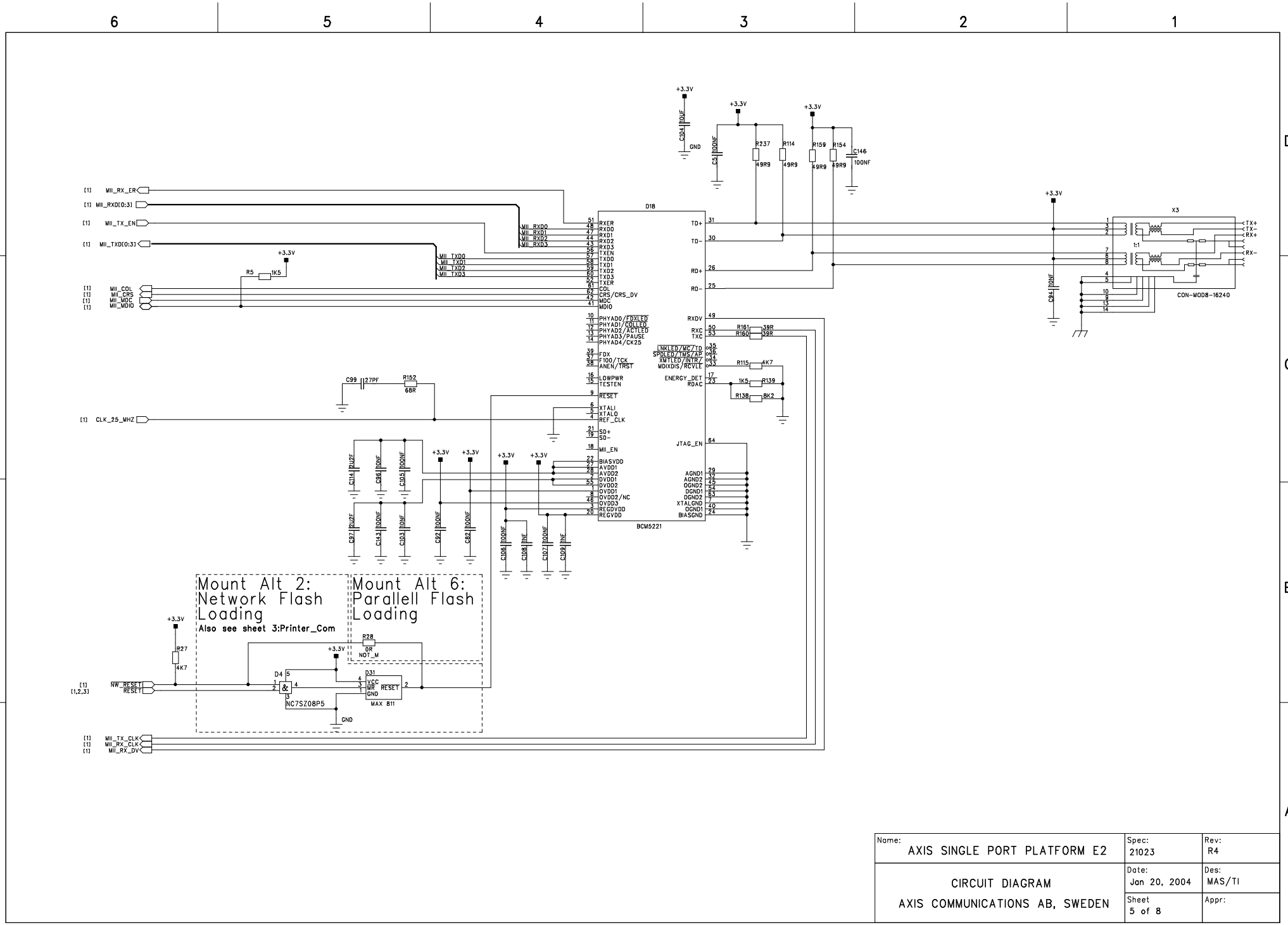

IC-ETRAX-100LX3-BGA256-18B16
D1
TEST BUTTON
STATUS
POWER
Mount Alt 7: Top LED (540 casing)
Mount Alt B: Front LED (5400 casing)
Mount Alt. 11: Side LED's for 55xx
L39 shall be Res OR 0603 when USB is used.
R97 shall be Ferrite 17933 when USB is used.
Serial port 0 and 1
Network interface
General port A
General port B
Bus status
DMA
Control signals
Bus signals
Data bus
Chip select
Adress bus
Test pins
PLL signals
ETRAX 100LX E3
MAX811
NC7SZ04
AXIS SINGLE PORT PLATFORM E2
CIRCUIT DIAGRAM
AXIS COMMUNICATIONS AB, SWEDEN
Spec: 21023
Rev: R4
Date: Jan 20, 2004
Des: MAS/TI
Sheet 1 of 8
Appr:



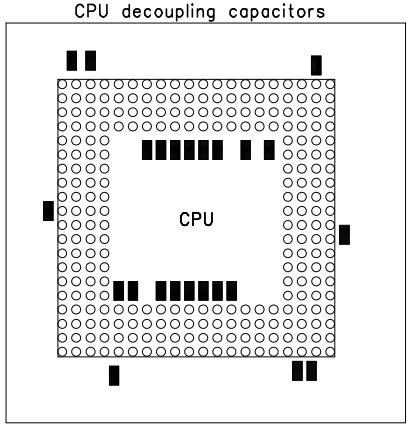


Name: AXIS SINGLE PORT PLATFORM E2	Spec: 21023	Rev: R4
CIRCUIT DIAGRAM	Date: Jan 20, 2004	Des: MAS/TI
AXIS COMMUNICATIONS AB, SWEDEN	Sheet 2 of 8	Appr:



Name: AXIS SINGLE PORT PLATFORM E2		Spec: 21023	Rev: R4
CIRCUIT DIAGRAM AXIS COMMUNICATIONS AB, SWEDEN		Date: Jan 20, 2004 Sheet 5 of 8	Des: MAS/TI Appr:

CPU decoupling capacitors



General design remarks

1. The PCB shall be 1.6mm thick and have max. 6 layers
2. The USB D+ and D− shall be routed with short and equal trace lengths
3. Route TD+/− and RD+/− with short and equal lengths traces. 50 Ohm impedance is recommended and shall be routed close to ground.
4. Add solder holes to CGND near the Centronics connector.

PCB layout priorities.

1. CLK signals net SDRAM_CLK, CLK_25_MHZ, MII_TX_CLK, MII_RX_CLK and CLK_IN shall be routed in between the GND and Vcc layer. Termination resisistor shall be closed to the source. The RC filter shall be close to the load. Signals in the other inner layer shall cross the CLK signals with 90 degrees.
2. No signal traces in near of the button S2.
3. GND vias shall be placed on the edge of the GND plane.
4. Parallell port signals shall be routed in the inner layer and shall not cross the adress and data bus.
5. Place GND under the holes on X1.
6. No spokes around the component pads.

Name: AXIS SINGLE PORT PLATFORM E2	Spec: 21023	Rev: R4
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